

NEC

NEC Electronics (Europe) GmbH

μ PD765A/ μ PD7265 SINGLE/DOUBLE DENSITY FLOPPY DISK CONTROLLER

Description

The μ PD765A is an LSI Floppy Disk Controller (FDC) chip which contains the circuitry and control functions for interfacing a processor to 4 floppy-disk drives. It is capable of supporting either IBM 3740 Single Density format (FM), or IBM System 34 Double Density format (MFM) including double-sided recording. The μ PD765A provides control signals which simplify the design of an external phase locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a floppy-disk interface.

The μ PD7265 is an addition to the FDC family that has been designed specifically for the Sony Micro Floppydisk® drive. The μ PD7265 is pin-compatible and electrically equivalent to the 765A but utilizes the Sony recording format. The μ PD7265 can read a diskette that has been formatted by the μ PD765A.

Hand-shaking signals are provided in the μ PD765A/ μ PD7265 which make DMA operation easy to incorporate with the aid of an external DMA Controller chip, such as the μ PD8257. The FDC will operate in either the DMA or non-DMA mode. In the non-DMA mode the FDC generates interrupts to the processor every time a data byte is to be transferred. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the FDC and DMA controllers.

There are 15 commands which the μ PD765A/ μ PD7265 will execute. Each of these commands requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

READ DATA	SCAN HIGH OR EQUAL	WRITE DELETED DATA
READ ID	SCAN LOW OR EQUAL	SEEK
SPECIFY	READ DELETED DATA	RECALIBRATE
READ TRACK	WRITE DATA	SENSE INTERRUPT STATUS
SCAN EQUAL	FORMAT TRACK	SENSE DRIVE STATUS

Features

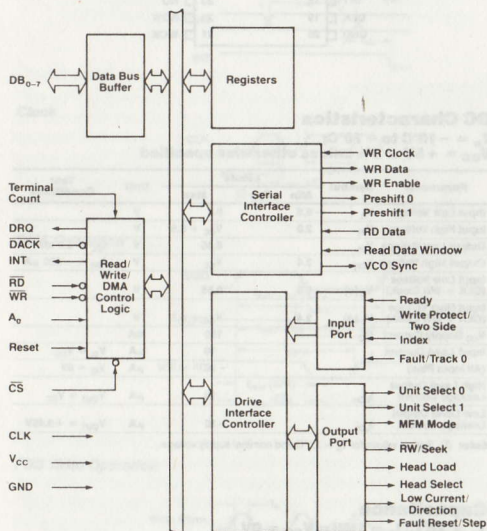
Address Mark detection circuitry is internal to the FDC which simplifies the phase locked loop and read electronics. The track stepping rate, head load time, and head unload time are user-programmable. The μ PD765A/ μ PD7265 offers additional features such as multitrack and multiside read and write commands and single and double density capabilities.

- ☐ Sony (EMCA) Compatible Recording Format (μ PD7265)
- ☐ IBM-compatible Format (Single and Double Density) (μ PD765A)
- ☐ Multisector and Multitrack Transfer Capability
- ☐ Drive Up to 4 Floppy or Micro Floppydisk® Drives
- ☐ Data Scan Capability—Will scan a single sector or an entire cylinder comparing byte-for-byte host memory and disk data

- ☐ Data Transfers in DMA or Non-DMA Mode
- ☐ Parallel Seek Operations on Up to Four Drives
- ☐ Compatible with μ PD8080/85, μ PD8086/88 and μ PD780 (Z80™) Microprocessors
- ☐ Single Phase Clock (8 MHz)
- ☐ +5V Only
- ☐ 40-Pin Plastic Package

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Micro Floppydisk® is a registered trademark of Sony Corporation.

Block Diagram



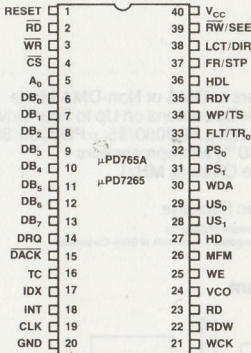
Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	-10°C to +70°C
Storage Temperature	-40°C to +125°C
All Output Voltages	-0.5 to +7V
All Input Voltages	-0.5 to +7V
Supply Voltage V _{CC}	-0.5 to +7V
Power Dissipation	1W

* COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

μPD765A/7265

Pin Configuration



DC Characteristics

$T_a = -10^\circ\text{C to } +70^\circ\text{C};$
 $V_{CC} = +5V \pm 5\%$ unless otherwise specified

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ ①	Max		
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		$V_{CC} + 0.5$	V	
Output Low Voltage	V_{OL}			0.45	V	$I_{OL} = 2.0 \text{ mA}$
Output High Voltage	V_{OH}	2.4		V_{CC}	V	$I_{OH} = -200 \mu\text{A}$
Input Low Voltage (CLK + WR Clock)	$V_{IL}(d)$	-0.5		0.65	V	
Input High Voltage (CLK + WR Clock)	$V_{IH}(d)$	2.4		$V_{CC} + 0.5$	V	
V_{CC} Supply Current	I_{CC}			150	mA	
Input Load Current (All Input Pins)	I_{LI}			10	μA	$V_{IN} = V_{CC}$
High Level Output Leakage Current	I_{LOH}			10	μA	$V_{OUT} = V_{CC}$
Low Level Output Leakage Current	I_{LOL}			-10	μA	$V_{OUT} = +0.45V$

Note: ① Typical values for $T_a = 25^\circ\text{C}$ and nominal supply voltage.

Capacitance

$T_a = 25^\circ\text{C}; f_c = 1\text{MHz}; V_{CC} = 0V$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Clock Input Capacitance	$C_{IN(d)}$			20	pF	All pins except pin under test tied to AC Ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

Pin Identification

No.	Symbol	Name	I/O	Connects To	Function
1	RST	Reset	I	Processor	Places FDC in idle state. Resets output lines to FDD to 0 (low). Does not affect SRT, HUT or HLT in Specify command. If RDY pin is held high during Reset, FDC will generate an interrupt within 1.024 msec. To clear this interrupt use Sense Interrupt Status command.
2	RD	Read	I ①	Processor	Control signal for transfer of data from FDC to Data Bus, when 0 (low).
3	WR	Write	I ①	Processor	Control signal for transfer of data to FDC via Data Bus, when 0 (low).
4	CS	Chip Select	I	Processor	IC selected when 0 (low), allowing RD and WR to be enabled.
5	A ₀	Data/Status Reg Select	I ①	Processor	Selects Data Reg ($A_0 = 1$) or Status Reg ($A_0 = 0$) contents of the FDC to be sent to Data Bus.
6-13	DB ₀ -DB ₇	Data Bus	I/O ①	Processor	Bidirectional 8-bit Data Bus.
14	DRQ	Data DMA Request	O	DMA	DMA Request is being made by FDC when DRQ = 1.
15	DACK	DMA Acknowledge	I	DMA	DMA cycle is active when 0 (low) and controller is performing DMA transfer.
16	TC	Terminal Count	I	DMA	Indicates the termination of a DMA transfer when 1 (high). It terminates data transfer during Read/Write Scan command in DMA or Interrupt mode.
17	IDX	Index	I	FDD	Indicates the beginning of a disk track.
18	INT	Interrupt	O	Processor	Interrupt Request generated by FDC.
19	CLK	Clock	I		Single phase 8 MHz square-wave clock.
20	GND	Ground			DC power return.
21	WCK	Write Clock	I		Write data rate to FDD. FM = 500 KHz; MFM = 1 MHz, with a pulse width of 250 ns for both FM and MFM.
22	RDW	Read Data Window	I	Phase Lock Loop	Generated by PLL, and used to sample data from FDD.
23	RDD	Read Data	I	FDD	Read data from FDD, containing clock and data bits.
24	VCO/ Sync	VCO/Sync	O	Phase Locked Loop	Inhibits VCO in PLL when 0 (low), enables VCO when 1.
25	WE	Write Enable	O	FDD	Enables write data into FDD.
26	MFM	MFM Mode	O	Phase Lock Loop	MFM mode when 1, FM mode when 0.
27	HD	Head Select	O	FDD	Head 1 selected when 1 (high). Head 0 selected when 0 (low).
28, 29	US ₁ , US ₀	Unit Select	O	FDD	FDD Unit selected.
30	WDA	Write Data	O	FDD	Serial clock and data bits to FDD.
31, 32	PS ₁ , PS ₀	Precompensation (preshift)	O	FDD	Write precompensation status during MFM mode. Determines early, late, and normal times.
33	FLT/TR ₀	Fault/Track 0	I	FDD	Senses FDD fault condition in Read/Write mode; and Track 0 condition in Seek mode.
34	WP/TS	Write Protect/Two Side	I	FDD	Senses Write Protect status in Read/Write mode; and Two-Side Media in Seek mode.
35	RDY	Ready	I	FDD	Indicates FDD is ready to send or receive data.
36	HDL	Head Load	O	FDD	Command which causes read/write head in FDD to contact diskette.
37	FR/STP	Flt Reset/Step	O	FDD	Resets fault FF in FDD in Read/Write mode, contains step pulses to move head to another cylinder in Seek mode.
38	LCT/DIR	Low Current/Direction	O	FDD	Lowers Write current on inner tracks in Read/Write mode, determines direction head will step in Seek mode. A fault reset pulse is issued at the beginning of each Read or Write command prior to the occurrence of the Head Load signal.
39	RW/SEEK	Read Write/Seek	O	FDD	When 1 (high) Seek mode selected and when 0 (low) Read/Write mode selected.
40	V _{CC}	+5V			DC power.

Note: ① Disabled when $\overline{CS} = 1$.

AC Characteristics

$T_a = -10^\circ\text{C to } 70^\circ\text{C}$;

$V_{CC} = +5\text{V} \pm 5\%$ unless otherwise specified

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ ^①	Max		
		120	125	500		
Clock Period	ϕCY		125		ns	8' FDD 5 1/4' FDD 3 1/2' Sony
Clock Active (High)	$\phi 0$	40			ns	
Clock Rise Time	ϕr			20	ns	
Clock Fall Time	ϕf			20	ns	
A_0 , CS, DACK Setup Time to RD \downarrow	t_{AR}	0			ns	
A_0 , CS, DACK Hold Time from RD \uparrow	t_{RA}	0			ns	
RD Width	t_{RR}	250			ns	
Data Access Time from RD \downarrow	t_{RD}			200	ns	$C_L = 100\text{ pF}$
DB to Float Delay Time from RD \uparrow	t_{DF}	20		100	ns	$C_L = 100\text{ pF}$
A_0 , CS, DACK Setup Time to WR \downarrow	t_{AW}	0			ns	
A_0 , CS, DACK Hold Time to WR \uparrow	t_{WA}	0			ns	
WR Width	t_{WW}	250			ns	
Data Setup Time to WR \uparrow	t_{DW}	150			ns	
Data Hold Time from WR \uparrow	t_{WD}	5			ns	
INT Delay Time from RD \uparrow	t_{RI}			500	ns	
INT Delay Time from WR \uparrow	t_{WI}			500	ns	
DRQ Cycle Time	t_{MCY}	13			μs	
DACK $\downarrow \rightarrow$ DRQ \downarrow Delay	t_{AM}			200	ns	
DRQ $\uparrow \rightarrow$ DACK \downarrow Delay	t_{MA}	200			ns	$\phi_{CY} = 125\text{ ns}$
DACK Width	t_{AA}	2			ϕ_{CY}	
TC Width	t_{TC}	1			ϕ_{CY}	
Reset Width	t_{RST}	14			ϕ_{CY}	
		4				MFM = 0 5 1/4"
		2				MFM = 1 5 1/4"
		2				MFM = 0 8"
		1				MFM = 1 8"
		2				MFM = 0 3 1/2" ③
		1				MFM = 1 3 1/2" ③
WCK Cycle Time	t_{CY}				μs	
WCK Active Time (High)	t_0	80	250	350	ns	
WCK Rise Time	t_r			20	ns	
WCK Fall Time	t_f			20	ns	
Preshift Delay Time from WCK \uparrow	t_{CP}	20		100	ns	
WCK $\uparrow \rightarrow$ WE \uparrow Delay	t_{CWE}	20		100	ns	
WDA Delay Time from WCK \uparrow	t_{CD}	20		100	ns	
RDD Active Time (High)	t_{RDD}	40			ns	
		4				MFM = 0 5 1/4"
		2				MFM = 1 5 1/4"
		2				MFM = 0 8"
		1				MFM = 1 8"
		2				MFM = 0 3 1/2"
		1				MFM = 1 3 1/2"
Window Cycle Time	t_{WCY}				μs	
Window Hold Time to/from RDD	t_{HWD}	15			ns	
US_{H1} Hold Time to RW/SEEK \uparrow	t_{US}	12			μs	
RW/SEEK Hold Time to LOW CURRENT/DIRECTION \downarrow	t_{SD}	7			μs	
LOW CURRENT/DIRECTION Hold Time to FAULT RESET/STEP \uparrow	t_{DST}	1.0			μs	
US_{H2} Hold Time from FAULT RESET/STEP \uparrow	t_{STU}	5.0			μs	8 MHz Clock Period ④
STEP Active Time (High)	t_{STP}	6	7	8	μs	④
STEP Cycle Time	t_{SC}	33	②	②	μs	④
FAULT RESET Active Time (High)	t_{FR}	8.0		10	μs	④
Write Data Width	t_{WDD}	T_0-50			ns	
US_{H3} Hold Time After SEEK	t_{SU}	15			μs	
Seek Hold Time from DIR	t_{OS}	30			μs	8 MHz Clock Period
DIR Hold Time after STEP	t_{STD}	24			μs	
Index Pulse Width	t_{IDX}	10			ϕ_{CY}	
RD \downarrow Delay from DRQ	t_{MR}	800			μs	
WR \downarrow Delay from DRQ	t_{MW}	250			μs	8 MHz Clock Period
WE or RD Response Time from DRQ \uparrow	t_{MRW}			12	μs	

Notes: ① Typical values for $T_a = 25^\circ\text{C}$ and nominal supply voltage.

② Under Software Control. The range is from 1 ms to 16 ms at 8 MHz clock period, and 2 to 32 ms at 4 MHz clock period.

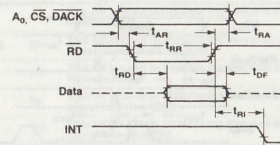
③ Sony Micro Floppydisk* 3 1/2" drive.

④ Double these values for a 4 MHz clock period.

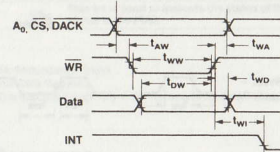
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Timing Waveforms

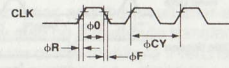
Processor Read Operation



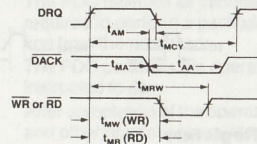
Processor Write Operation



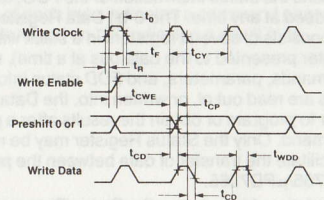
Clock



DMA Operation



FDD Write Operation

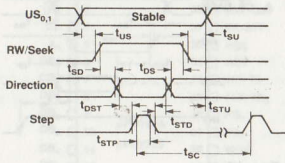


	Preshift 0	Preshift 1
Normal	0	0
Late	0	1
Early	1	0
Invalid	1	1

μPD765A/7265

Timing Waveforms (Cont.)

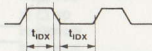
Seek Operation



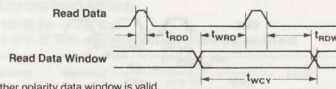
FLT Reset

Fault Reset =
File Unsafe Reset

Index



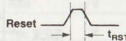
FDD Read Operation



Note: Either polarity data window is valid.

Terminal Count

Reset



Internal Registers

The μPD765A/μPD7265 contains two registers which may be accessed by the main system processor: a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (which actually consists of several registers in a stack with only one register presented to the data bus at a time), stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command. Only the Status Register may be read and used to facilitate the transfer of data between the processor and μPD765/μPD7265.

The relationship between the Status/Data registers and the signals RD, WR, and A₀ is shown below.

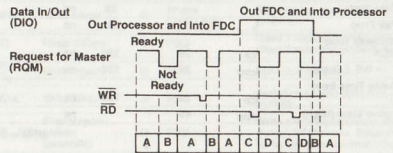
A ₀	RD	WR	Function
0	0	1	Read Main Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

Internal Registers (Cont.)

The bits in the Main Status Register are defined as follows:

No.	Bit	Symbol	Description
DB ₀	FDD 0 Busy	D ₀ B	FDD number 0 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB ₁	FDD 1 Busy	D ₁ B	FDD number 1 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB ₂	FDD 2 Busy	D ₂ B	FDD number 2 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB ₃	FDD 3 Busy	D ₃ B	FDD number 3 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB ₄	FDC Busy	CB	A read or write command is in process. FDC will not accept any other command.
DB ₅	Execution Mode	EXM	This bit is set only during execution phase in non-DMA mode. When DB ₅ goes low, execution phase has ended and result phase has started. It operates only during non-DMA mode of operation.
DB ₆	Data Input/Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = 1, then transfer is from Data Register to the processor. If DIO = 0, then transfer is from the processor to Data Register.
DB ₇	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor.

The DIO and RQM bits in the Status Register indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last RD or WR during a command or result phase and DIO and RQM getting set or reset is 12 μs. For this reason every time the Main Status Register is read the CPU should wait 12 μs. The maximum time from the trailing edge of the last RD in the result phase to when DB₄ (FDC busy) goes low is 12 μs.



- Notes: ① — Data register ready to be written into by processor.
② — Data register not ready to be written into by processor.
③ — Data register ready for next data byte to be read by processor.
④ — Data register not ready to be read by processor.

Status Register Identification

Bit			Description
No.	Name	Symbol	
Status Register 0			
D ₇	Interrupt Code	IC	D ₇ = 0 and D ₆ = 0 Normal Termination of command, (NT). Command was completed and properly executed.
			D ₇ = 0 and D ₆ = 1 Abnormal Termination of command, (AT). Execution of command was started but was not successfully completed.
			D ₇ = 1 and D ₆ = 0 ¹⁾ Invalid Command Issue, (IC). Command which was issued was never started.
D ₆			D ₇ = 1 and D ₆ = 1 Abnormal Termination because during command execution the ready signal from FDD changed state.
D ₅	Seek End	SE	When the FDC completes the SEEK command, this flag is set to 1 (high).
D ₄	Equipment Check	EC	If a fault signal is received from the FDD, or if the Track 0 signal fails to occur after 77 step pulses (Recalibrate Command) then this flag is set.
D ₃	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single-sided drive, then this flag is set.
D ₂	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D ₁	Unit Select 1	US ₁	These flags are used to indicate a Drive Unit Number at Interrupt.
D ₀	Unit Select 0	US ₀	
Status Register 1			
D ₇	End of Cylinder	EN	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D ₆			Not used. This bit is always 0 (low).
D ₅	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D ₄	Overrun	OR	If the FDC is not serviced by the host system during data transfers within a certain time interval, this flag is set.
D ₃			Not used. This bit always 0 (low).
D ₂	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN command, if the FDC cannot find the sector specified in the IDR Register, this flag is set.
			During execution of the READ ID command, if the FDC cannot read the ID field without an error, then this flag is set.
D ₁	Not Writable	NW	During execution of the READ A cylinder command, if the starting sector cannot be found, then this flag is set.
			During execution of WRITE DATA, WRITE DELETED DATA or Format A cylinder command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D ₀	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.
			If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in data field) of Status Register 2 is set.
Status Register 2			
D ₇			Not used. This bit is always 0 (low).
D ₆	Control Mark	CM	During execution of the READ DATA or SCAN command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set.
D ₅	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D ₄	Wrong Cylinder	WC	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D ₃	Scan Equal Hit	SH	During execution of the SCAN command, if the condition of "equal" is satisfied, this flag is set.
D ₂	Scan Not Satisfied	SN	During execution of the SCAN command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D ₁	Bad Cylinder	BC	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FF ₁₆ , then this flag is set.
D ₀	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.

Status Register Identification (Cont.)

Bit			Description
No.	Name	Symbol	
Status Register 3			
D ₇	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D ₆	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D ₅	Ready	RY	This bit is used to indicate the status of the Ready signal from the FDD.
D ₄	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D ₃	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D ₂	Head Address	HD	This bit is used to indicate the status of the Side Select signal to the FDD.
D ₁	Unit Select 1	US ₁	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D ₀	Unit Select 0	US ₀	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

Notes: ① CRC = Cyclic Redundancy Check
 ② IDR = Internal Data Register
 ③ Cylinder (C) is described more fully in the Command Symbol Description on page 7.

Command Sequence

The μPD765A/μPD7265 is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor, and the result after execution of the command may also be a multibyte transfer back to the processor. Because of this multibyte interchange of information between the μPD765A/μPD7265 and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase:	The FDC receives all information required to perform a particular operation from the processor.
Execution Phase:	The FDC performs the operation it was instructed to do.
Result Phase:	After completion of the operation, status and other housekeeping information are made available to the processor.

Following are shown the required preset parameters and results for each command. Most commands require 9 command bytes and return 7 bytes during the result phase. The "W" to the left of each byte indicates a command phase byte to be written, and an "R" indicates a result byte.

Instruction Set ① ②

Data Bus										
Phase	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Remarks
Read Data										
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US ₁	US ₀	③
	W	←	←	←	←	←	←	←	←	Sector ID information prior to command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	←	←	←	←	←	←	←	←	EOT
	W	←	←	←	←	←	←	←	←	GPL
	W	←	←	←	←	←	←	←	←	DTL
	W	←	←	←	←	←	←	←	←	
Execution										
Result	R	←	←	←	←	←	←	←	←	Status information after command execution
	R	←	←	←	←	←	←	←	←	ST 0
	R	←	←	←	←	←	←	←	←	ST 1
	R	←	←	←	←	←	←	←	←	ST 2
	R	←	←	←	←	←	←	←	←	Sector ID information after command execution
	R	←	←	←	←	←	←	←	←	H
	R	←	←	←	←	←	←	←	←	N
Read Deleted Data										
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US ₁	US ₀	
	W	←	←	←	←	←	←	←	←	Sector ID information prior to command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	←	←	←	←	←	←	←	←	EOT
	W	←	←	←	←	←	←	←	←	GPL
	W	←	←	←	←	←	←	←	←	DTL
	W	←	←	←	←	←	←	←	←	
Execution										
Result	R	←	←	←	←	←	←	←	←	Status information after command execution
	R	←	←	←	←	←	←	←	←	ST 0
	R	←	←	←	←	←	←	←	←	ST 1
	R	←	←	←	←	←	←	←	←	ST 2
	R	←	←	←	←	←	←	←	←	Sector ID information after command execution
	R	←	←	←	←	←	←	←	←	H
	R	←	←	←	←	←	←	←	←	N
Write Data										
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US ₁	US ₀	
	W	←	←	←	←	←	←	←	←	Sector ID information prior to command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	←	←	←	←	←	←	←	←	EOT
	W	←	←	←	←	←	←	←	←	GPL
	W	←	←	←	←	←	←	←	←	DTL
	W	←	←	←	←	←	←	←	←	
Execution										
Result	R	←	←	←	←	←	←	←	←	Status information after command execution
	R	←	←	←	←	←	←	←	←	ST 0
	R	←	←	←	←	←	←	←	←	ST 1
	R	←	←	←	←	←	←	←	←	ST 2
	R	←	←	←	←	←	←	←	←	Sector ID information after command execution
	R	←	←	←	←	←	←	←	←	H
	R	←	←	←	←	←	←	←	←	N

Notes: ① Symbols used in this table are described at the end of this section.

② A₀ should equal binary 1 for all operations.

③ X = Don't care, usually made to equal binary 0.

Instruction Set

Phase		R/W	Data Bus								Remarks
			D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
			Write Deleted Data								
Command	W	MT	MF	0	0	1	0	0	1	Command Codes	
	W	X	X	X	X	X	HD	US ₁	US ₀		
	W	←	←	←	←	←	←	←	←		Sector ID information prior to command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	←	←	←	←	←	←	←	←		EOT
	W	←	←	←	←	←	←	←	←		GPL
	W	←	←	←	←	←	←	←	←		DTL
	W	←	←	←	←	←	←	←	←		
Execution											
Data transfer between the FDD and main system											
Result	R	←	←	←	←	←	←	←	←	Status information after command execution	
	R	←	←	←	←	←	←	←	←		ST 0
	R	←	←	←	←	←	←	←	←		ST 1
	R	←	←	←	←	←	←	←	←		ST 2
	R	←	←	←	←	←	←	←	←		C
	R	←	←	←	←	←	←	←	←		Sector ID information after command execution
	R	←	←	←	←	←	←	←	←		H
R	←	←	←	←	←	←	←	←	N		
Read A Track											
Command	W	0	MF	SK	0	0	0	1	0	Command Codes	
	W	X	X	X	X	X	HD	US ₁	US ₀		
	W	←	←	←	←	←	←	←	←		Sector ID information prior to command execution
	W	←	←	←	←	←	←	←	←		EOT
	W	←	←	←	←	←	←	←	←		GPL
	W	←	←	←	←	←	←	←	←		DTL
	W	←	←	←	←	←	←	←	←		
Execution											
Data transfer between the FDD and main system. FDC reads all data fields from index hole to EOT.											
Result	R	←	←	←	←	←	←	←	←	Status information after command execution	
	R	←	←	←	←	←	←	←	←		ST 0
	R	←	←	←	←	←	←	←	←		ST 1
	R	←	←	←	←	←	←	←	←		ST 2
	R	←	←	←	←	←	←	←	←		C
	R	←	←	←	←	←	←	←	←		Sector ID information after command execution
	R	←	←	←	←	←	←	←	←		H
R	←	←	←	←	←	←	←	←	N		
Read ID											
Command	W	0	MF	0	0	1	0	1	0	Command Codes	
	W	X	X	X	X	X	HD	US ₁	US ₀		
	W	←	←	←	←	←	←	←	←		The first correct ID information on the cylinder is stored in Data Register.
	W	←	←	←	←	←	←	←	←		EOT
	W	←	←	←	←	←	←	←	←		GPL
	W	←	←	←	←	←	←	←	←		DTL
	W	←	←	←	←	←	←	←	←		
Execution											
The first correct ID information on the cylinder is stored in Data Register.											
Result	R	←	←	←	←	←	←	←	←	Status information after command execution	
	R	←	←	←	←	←	←	←	←		ST 0
	R	←	←	←	←	←	←	←	←		ST 1
	R	←	←	←	←	←	←	←	←		ST 2
	R	←	←	←	←	←	←	←	←		C
	R	←	←	←	←	←	←	←	←		Sector ID information read during Execution phase from Floppy Disk.
	R	←	←	←	←	←	←	←	←		H
R	←	←	←	←	←	←	←	←	N		
Format A Track											
Command	W	0	MF	0	0	1	1	0	1	Command Codes	
	W	X	X	X	X	X	HD	US ₁	US ₀		
	W	←	←	←	←	←	←	←	←		Bytes/Sector
	W	←	←	←	←	←	←	←	←		Sectors/Track
	W	←	←	←	←	←	←	←	←		Gap 3
	W	←	←	←	←	←	←	←	←		Filler byte
	W	←	←	←	←	←	←	←	←		
Execution											
FDC formats an entire track.											
Result	R	←	←	←	←	←	←	←	←	Status information after command execution	
	R	←	←	←	←	←	←	←	←		ST 0
	R	←	←	←	←	←	←	←	←		ST 1
	R	←	←	←	←	←	←	←	←		ST 2
	R	←	←	←	←	←	←	←	←		C
	R	←	←	←	←	←	←	←	←		In this case, the ID information has no meaning.
	R	←	←	←	←	←	←	←	←		H
R	←	←	←	←	←	←	←	←	N		
Scan Equal											
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes	
	W	X	X	X	X	X	HD	US ₁	US ₀		
	W	←	←	←	←	←	←	←	←		Sector ID information prior to command execution
	W	←	←	←	←	←	←	←	←		EOT
	W	←	←	←	←	←	←	←	←		GPL
	W	←	←	←	←	←	←	←	←		STP
	W	←	←	←	←	←	←	←	←		
Execution											
Data compared between the FDD and main system											
Result	R	←	←	←	←	←	←	←	←	Status information after command execution	
	R	←	←	←	←	←	←	←	←		ST 0
	R	←	←	←	←	←	←	←	←		ST 1
	R	←	←	←	←	←	←	←	←		ST 2
	R	←	←	←	←	←	←	←	←		C
	R	←	←	←	←	←	←	←	←		Sector ID information after command execution
	R	←	←	←	←	←	←	←	←		H
R	←	←	←	←	←	←	←	←	N		

Instruction Set

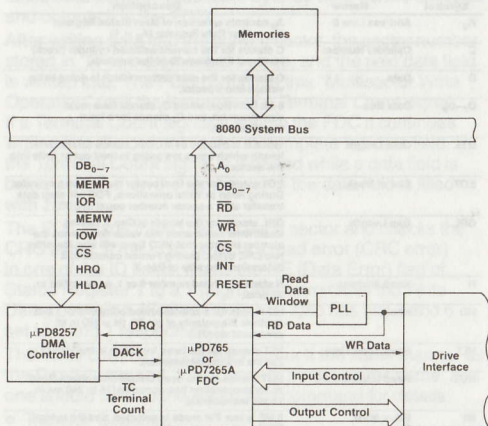
Data Bus											Remarks	
Phase	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀			
Scan Low or Equal												
Command	W	MT	MF	SK	1	1	0	0	1	Command Codes		
	W	X	X	X	X	X	HD	US ₁	US ₀	Sector ID information prior to command execution		
	W					C						
	W					H						
	W					N						
	W					EOT						
	W					GPL						
Execution	W					STP						
	Data compared between the FDD and main system											
Result	R					ST 0	Status information after command execution					
	R					ST 1						
	R					ST 2						
	R					C	Sector ID information after command execution					
	R					H						
	R					N						
Scan High or Equal												
Command	W	MT	MF	SK	1	1	1	0	1	Command Codes		
	W	X	X	X	X	X	HD	US ₁	US ₀	Sector ID information prior to command execution		
	W					C						
	W					H						
	W					N						
	W					EOT						
	W					GPL						
Execution	W					STP						
	Data compared between the FDD and main system											
Result	R					ST 0	Status information after command execution					
	R					ST 1						
	R					ST 2						
	R					C	Sector ID information after command execution					
	R					H						
	R					N						
Recalibrate												
Command	W	0	0	0	0	0	1	1	1	Command Codes		
	W	X	X	X	X	X	0	US ₁	US ₀			
Execution												
Head retracted to Track 0												
Sense Interrupt Status												
Command	W	0	0	0	0	1	0	0	0	Command Codes		
	W	X	X	X	X	X	0	US ₁	US ₀			
Result	R					STO	Status information about the FDC at the end of seek operation					
	R					PCN						
Specify												
Command	W	0	0	0	0	0	0	1	1	Command Codes		
	W	SRT				HUT						
	W	HLT				ND						
Sense Drive Status												
Command	W	0	0	0	0	0	1	0	0	Command Codes		
	W	X	X	X	X	X	HD	US ₁	US ₀			
Result	R					ST 3	Status information about FDD					
Seek												
Command	W	0	0	0	0	1	1	1	1	Command Codes		
	W	X	X	X	X	X	HD	US ₁	US ₀			
	W					NCN						
Execution												
Head is positioned over proper cylinder on diskette.												
Invalid												
Command	W					Invalid Codes	Invalid Command Codes (NoOp—FDC goes into Standby state.)					
	W											
Result	R					ST 0	ST 0 = 80 ₍₁₆₎					
	R											

Command Symbol Description

Symbol	Name	Description
A ₀	Address Line 0	A ₀ controls selection of Main Status Register (A ₀ = 0) or Data Register (A ₀ = 1)
C	Cylinder Number	C stands for the current/selected cylinder (track) numbers 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a sector.
D ₇ -D ₀	Data Bus	8-bit Data Bus, where D ₇ stands for a most significant bit, and D ₀ stands for a least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the sector.
EOT	End of Track	EOT stands for the final sector number on a cylinder. During Read or Write operations, FDC will stop data transfer after a sector number equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCO Sync will stay low after two CRC bytes. During Format command it determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a Read or Write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multitrack	If MT is high, a Multitrack operation is performed. If MT = 1 after finishing Read/Write operation on side 0, FDC will automatically start searching for sector 1 on side 1.
N	Number	N stands for the Number of data bytes written in a sector.
NCN	New Cylinder Number	NCN stands for a New Cylinder Number which is going to be reached as a result of the Seek operation. desired position of head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA mode.
PCN	Present Cylinder Number	PCN stands for the cylinder number at the completion of Sense Interrupt Status command. position of Head at present time.
R	Record	R stands for the sector number which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD (1 to 16 ms in 1 ms increments). Stepping Rate applies to all drives (F ₍₁₆₎ = 1 ms, E ₍₁₆₎ = 2 ms, etc.).
ST0	Status 0	ST 0-3 stands for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A ₀ = 0). ST 0-3 may be read only after a command has been executed and contains information relevant to that particular command.
ST1	Status 1	
ST2	Status 2	
ST3	Status 3	
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
US ₀ , US ₁	Unit Select	US stands for a selected drive number 0 or 1.

μPD765A/7265

System Configuration



Processor Interface

During Command or Result phases the Main Status Register (described earlier) must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data read or written to the Data Register, CPU should wait for 12μs before reading Main Status Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the μPD765A/μPD7265. Many of the commands require multiple bytes and, as a result, the Main Status Register must be read prior to each byte transfer to the μPD765A/μPD7265. On the other hand, during the Result phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note that this reading of the Main Status Register before each byte transfer to the μPD765A/μPD7265 is required only in the Command and Result phases, and *not* during the Execution phase.

During the Execution phase, the Main Status Register need not be read. If the μPD765A/μPD7265 is in the non-DMA mode, then the receipt of each data byte (if μPD765A/μPD7265 is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal (RD = 0) or Write signal (WR = 0) will clear the Interrupt as well as output the data onto the data bus. If the processor cannot handle Interrupts fast enough (every 13 μs for the MFM mode and 27 μs for the FM mode), then it may poll the Main Status Register and bit D7 (RQM) functions as the Interrupt signal. If a Write command is in process then the WR signal negates the reset to the Interrupt signal.

Note that in the non-DMA mode it is necessary to examine the Main Status Register to determine the cause of the interrupt, since it could be a data interrupt or a command termination interrupt, either normal or abnormal.

If the μPD765A/μPD7265 is in the DMA mode, no Interrupts are generated during the Execution phase. The μPD765A/μPD7265 generates DRQs (DMA Requests) when each byte of data is available. The DMA Controller

responds to this request with both a $\overline{\text{DACK}} = 0$ (DMA Acknowledge) and an $\text{RD} = 0$ (Read signal). When the DMA Acknowledge signal goes low ($\overline{\text{DACK}} = 0$), then the DMA Request is cleared ($\text{DRQ} = 0$). If a Write command has been issued then a WR signal will appear instead of RD. After the Execution phase has been completed (Terminal Count has occurred) or the EOT sector read/written, then an Interrupt will occur ($\text{INT} = 1$). This signifies the beginning of the Result phase. When the first byte of data is read during the Result phase, the Interrupt is automatically cleared ($\text{INT} = 0$).

The RD or WR signals should be asserted while $\overline{\text{DACK}}$ is true. The CS signal is used in conjunction with RD and WR as a gating function during programmed I/O operations. CS has no effect during DMA operations. If the non-DMA mode is chosen, the $\overline{\text{DACK}}$ signal should be pulled up to V_{CC} .

It is important to note that during the Result phase all bytes shown in the Command Table must be read. The Read Data command, for example, has seven bytes of data in the Result phase. All seven bytes must be read in order to successfully complete the Read Data command. The μPD765A/μPD7265 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result phase.

The μPD765A/μPD7265 contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are available only during the Result phase and may be read only after completing a command. The particular command that has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the μPD765A/μPD7265 to form the Command phase and are read out of the μPD765A/μPD7265 in the Result phase must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result phases is allowed. After the last byte of data in the Command phase is sent to the μPD765A/μPD7265, the Execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result phase, the command is automatically ended and the μPD765A/μPD7265 is ready for a new command.

Polling Feature of the μPD765A/μPD7265

After Reset has been sent to the μPD765A/μPD7265, the Unit Select lines US_0 and US_1 will automatically go into a polling mode. In between commands (and between step pulses in the Seek command) the μPD765A/μPD7265 polls all four FDDs looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing), then the μPD765A/μPD7265 will generate an interrupt. When Status Register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the Ready line by the μPD765A/μPD7265 occurs continuously between commands, thus notifying the processor which drives are on or off line. Each drive is polled every 1.024 ms except during the Read/Write commands. When used with a 4 MHz clock for interfacing to minifloppies, the polling rate is 2.048 ms.

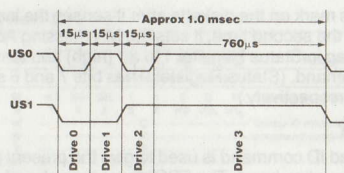


figure 1. (polling feature)

Read Data

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation". The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time that the DACK for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command. The amount of data which can be handled with a single command to the FDC depends upon MT (multitrack), MF (MFM/FM), and N (Number of Bytes/Sector). Table 1 below shows the Transfer Capacity.

Transfer Capacity

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskettes
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and

depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexidecimal.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 μs in the FM Mode, and every 13 μs in the MFM Mode, or the FDC sets the OR (Overrun) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 2 shows the values for C, H, R, and N, when the processor terminates the Command.

Functional Description of Commands

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	C + 1	NC	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
1	0	Equal to EOT	C + 1	NC	R = 01	NC
	0	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	NC	LSB	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	LSB	R = 01	NC

Notes: NC (No Change). The same value as the one at the beginning of command execution. LSB (Least Significant Bit). The least significant bit of H is complemented.

Write Data

A set of nine (9) bytes is required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID fields. When all four bytes loaded during the command (C, H, R, N) match

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the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus and outputs it to the FDD.

After writing data into the current sector, the sector number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multisector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (CRC error) in one of the ID fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high) and terminates the Write Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write command operates in much the same manner as the Read command. The following items are the same, and one should refer to the Read Data command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the data bus, must occur every 27 μs in the FM mode and every 13 μs in the MFM mode. If the time interval between data transfers is longer than this, then the FDC sets the OR (Overrun) flag in Status Register 1 to a 1 (high) and terminates the Write Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

Write Deleted Data

This command is the same as the Write Data command except a Deleted Data Address mark is written at the beginning of the data field instead of the normal Data Address mark.

Read Deleted Data

This command is the same as the Read Data command except that when the FDC detects a Data Address mark at the beginning of a data field (and SK = 0 (low)), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address mark and reads the next sector.

Read A Track

This command is similar to the Read Data command except that this is a continuous Read operation where the entire data field from each of the sectors is read. Immediately after sensing the index hole, the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multitrack or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT. If the FDC does not find an ID

Address mark on the diskette after it senses the index hole for the second time, it sets the MA (Missing Address mark) flag in Status Register 1 to a 1 (high) and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

Read ID

The Read ID command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID Address mark is found on the diskette before the index hole is encountered for the second time, then the MA (Missing Address mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

Format A Track

The Format command allows an entire track to be formatted. After the index hole is detected, data is written on the diskette; Gaps, Address marks, ID fields and data fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) format are recorded. The particular format which will be written is controlled by the values programmed into N (Number of bytes/sector), SC (Sectors/Cylinder), GPL (Gap Length), and D (Data pattern) which are supplied by the processor during the Command phase. The data field is filled with the byte of data stored in D. The ID field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder number), H (Head number), R (Sector number) and N (Number of bytes/sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the μPD765A/μPD7265 for each sector on the track. If FDC is set for the DMA mode, it will issue four DMA requests per sector. If it is set for the Interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R, and N loads for each sector. The contents of the R register are incremented by 1 after each sector is formatted; thus, the R register contains a value of R when it is read during the Result phase. This incrementing and formatting continues for the whole track until the FDC detects the index hole for the second time, whereupon it terminates the command.

If a Fault signal is received from the FDD at the end of a Write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high) and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a Ready signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respectively.

Table 1 shows the relationship between N, SC, and GPL for various sector sizes.

Functional Description of Commands (Cont.)

Format	Sector Size	N	SC	GPL ^①	GPL ^{②③}
8" Standard Floppy					
FM Mode	128 bytes/sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode ^④	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5¼" Minifloppy					
FM Mode	128 bytes/sector	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode ^④	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3½" Sony Micro Floppydisk^⑤					
FM Mode	128 bytes/sector	0	0F	07	1B
	256	1	09	0E	2A
	512	2	05	1B	3A
MFM Mode ^④	256	1	0F	0E	36
	512	2	09	1B	54
	1024	3	05	35	74

Table 1

Notes: ① Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sectors.
 ② Suggested values of GPL in format command.
 ③ All values except sector size are hexadecimal.
 ④ In MFM mode FDC cannot perform a Read/Write/format operation with 128 bytes/sector. (N = 00)

Scan Commands

The Scan commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. The hexadecimal byte of FF either from memory or from FDD can be used as a mask byte because it always meets the condition of the comparison. One's complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented ($R + STP \rightarrow R$), and the scan operation is continued. The scan operation continues until one of the following conditions occur: the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met, then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high) and terminates the Scan command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high) and terminates the Scan command. The receipt of a Terminal Count signal from the processor or DMA controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process and then to terminate the command. Table 2

shows the status of bits SH and SN under various conditions of Scan.

Status Register 2			
Command	Bit 2 = SN	Bit 3 = SH	Comments
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
	0	1	$D_{FDD} = D_{Processor}$
Scan Low or Equal	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} > D_{Processor}$
	0	1	$D_{FDD} = D_{Processor}$
Scan High or Equal	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} < D_{Processor}$
	0	1	$D_{FDD} = D_{Processor}$

Table 2

If the FDC encounters a Deleted Data Address mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address mark and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02) sectors are read or the MT (Multitrack) is programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26 and the Scan command is started at sector 21, the following will happen: Sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the index hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan command would be completed in a normal manner.

During the Scan command, data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Overrun) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM mode) or 13 μs (MFM mode). If an Overrun occurs, the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

Seek

The Read/Write head within the FDD is moved from cylinder to cylinder under control of the Seek command. FDC has four independent Present Cylinder Registers for each drive. They are cleared only after the Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference, performs the following operations:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In)
 PCN > NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued. (Step Out)

The rate at which Step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each Step pulse is issued NCN is compared against PCN, and when NCN = PCN, the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits D_3B-D_0B in the Main Status Register are set during the Seek operation and are cleared by the Sense Interrupt Status command.

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During the command phase of the Seek operation the FDC is in the FDC Busy state, but during the execution phase it is in the Nonbusy state. While the FDC is in the Nonbusy state, another Seek command may be issued, and in this manner parallel Seek operations may be done on up to four drives at once. No other command can be issued for as long as the FDC is in the process of sending step pulses to any drive.

If an FDD is in a Not Ready state at the beginning of the command execution phase or during the Seek operation, then the NR (Not Ready) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

If the time to write three bytes of Seek command exceeds 150μs, the timing between the first two step pulses may be shorter than set in the Specify command by as much as 1ms.

Recalibrate

The function of this command is to retract the Read/Write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and step pulses are issued. When the Track 0 signal goes high, the SE (Seek End) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 step pulses have been issued, the FDC sets the SE (Seek End) and EC (Equipment Check) flags of Status Register 0 to both 1s (highs) and terminates the command after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the Ready signal, as described in the Seek command, also applies to the Recalibrate command. If the Diskette has more than 77 tracks, then Recalibrate command should be issued twice, in order to position the Read/Write head to the Track 0.

Sense Interrupt Status

An Interrupt signal is generated by the FDC for one of the following reasons:

- Upon entering the Result phase of:
 - Read Data command
 - Read A Track command
 - Read ID command
 - Read Deleted Data command
 - Write Data command
 - Format A Cylinder command
 - Write Deleted Data command
 - Scan commands
- Ready Line of FDD changes state
- End of Seek or Recalibrate command
- During Execution phase in the non-DMA mode

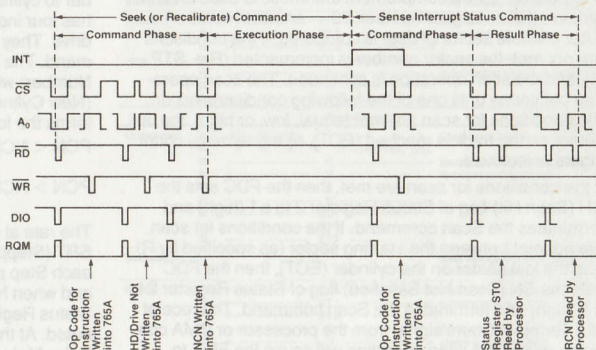
Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in non-DMA mode, DB5 in the Main Status Register is high. Upon entering the Result phase this bit gets cleared. Reasons 1 and 4 do not require Sense Interrupt Status commands. The interrupt is cleared by Reading/Writing data to the FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status command. This command when issued resets the Interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

Seek End Bit 5	Interrupt Code			Cause
	Bit 6	Bit 7	Bit 7	
0	1	1	1	Ready Line changed state, either polarity
1	0	0	0	Normal Termination of Seek or Recalibrate command
1	1	0	0	Abnormal Termination of Seek or Recalibrate command

Table 3

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no result phase. When the disk drive has reached the desired head position the μPD765A/μPD7265 will set the Interrupt line true. The host CPU must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt, which could be Seek End or a change in ready status from one of the drives. A graphic example is shown:

Seek, Recalibrate, and Sense Interrupt Status



Specify

The Specify command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the execution phase of one of the Read/Write commands to the head unload state. This timer is programmable from 16 to 240ms in increments of 16ms (01 = 16ms, 02 = 32ms... 0F₁₆ = 240ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1ms, E = 2ms, D = 3ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2ms, 02 = 4ms, 03 = 6ms... 7F = 254ms).

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8MHz clock; if the clock was reduced to 4MHz (minifloppy application) then all time intervals are increased by a factor of 2.

The choice of a DMA or non-DMA operation is made by the ND (Non-DMA) bit. When this bit is high (ND = 1) the Non-DMA mode is selected, and when ND = 0 the DMA mode is selected.

Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

Invalid

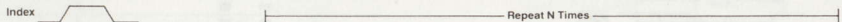
If an Invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated by the μPD765A/μPD765 during this condition. Bits 6 and 7 (DIO and RQM) in the Main Status Register are both high (1), indicating to the processor that the μPD765A/μPD765 is in the Result phase and the contents of Status Register 0 (ST0) must be read. When the processor reads Status Register 0 it will find an 80 hex, indicating an Invalid command was received.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC will consider the next command to be an Invalid command.

In some applications the user may wish to use this command as a No-Op command to place the FDC in a standby or No Operation state.

μPD765A (FM Mode)

GAP 4a 40x FF	SYNC 6x 00	IAM FC	GAP 1 26x FF	SYNC 6x 00	IDAM FE	C Y L	H D	S E C	N O	C R C	GAP 2 11x FF	SYNC 6x 00	DATA AM FB or F8	DATA	C R C	GAP 3	GAP 4b
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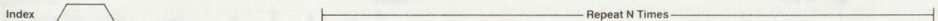
μPD765 (FM Mode)

GAP 1 16x FF	SYNC 6x 00	IDAM FE	C Y L	H D	S E C	N O	C R C	GAP 2 11x FF	SYNC 6x 00	DATA AM FB or F8	DATA	C R C	GAP 3	GAP 4
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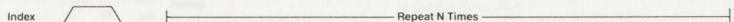
μPD765A (MFM Mode)

GAP 4a 80x 4E	SYNC 12x 00	IAM		GAP 1 50x 4E	SYNC 12x 00	IDAM		C Y L	H D	S E C	N O	C R C	GAP 2 22x 4E	SYNC 12x 00	DATA AM		DATA	C R C	GAP 3	GAP 4b
		3x C2	FC			3x A1	FE								3x A1	FB F8				



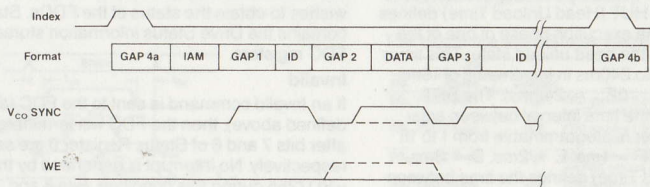
μPD765 (MFM Mode)

GAP 1 32x 4E	SYNC 12x 00	IDAM		C Y L	H D	S E C	N O	C R C	GAP 2 22x 4E	SYNC 12x 00	DATA AM		DATA	C R C	GAP 3	GAP 4
		3x A1	FE								3x A1	FB F8				

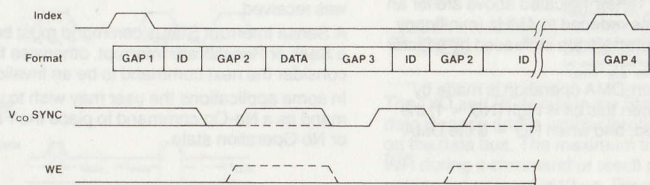


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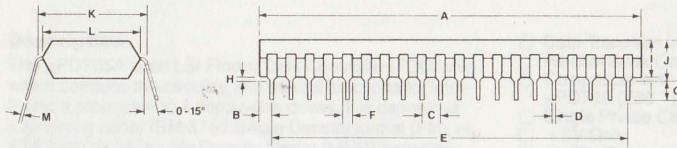
Note: — Read
 - - - Write

Notes: It is suggested that the user refer to the following application notes:
 : #8 — for an example of an actual interface, as well as a "theoretical" data separator.
 : #10 — for a well documented example of a working phase — locked loop.

Package Outlines

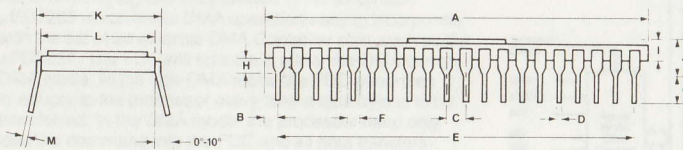
40 PIN

μPD765AC/7265C Plastic



Item	Millimeters	Inches
A	51.5 max	2.028 max
B	1.62 max	0.064 max
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.2 min	0.047 min
G	2.54 min	0.10 min
H	0.5 min	0.019 min
I	5.22 max	0.206 max
J	5.72 max	0.225 max
K	15.24 typ	0.600 typ
L	13.2 typ	0.520 typ
M	0.25 + 0.1 - 0.05	0.010 + 0.004 - 0.002

μPD765AD/7265D Ceramic



Item	Millimeters	Inches
A	51.5 max	2.03 max
B	1.62 max	0.06 max
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 min	0.04 min
G	3.2 min	0.13 min
H	1.0 min	0.04 min
I	3.5 max	0.14 max
J	4.5 max	0.18 max
K	15.24 typ	0.6 typ
L	14.93 typ	0.59 typ
M	0.25 ± 0.05	0.01 ± 0.0019

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