

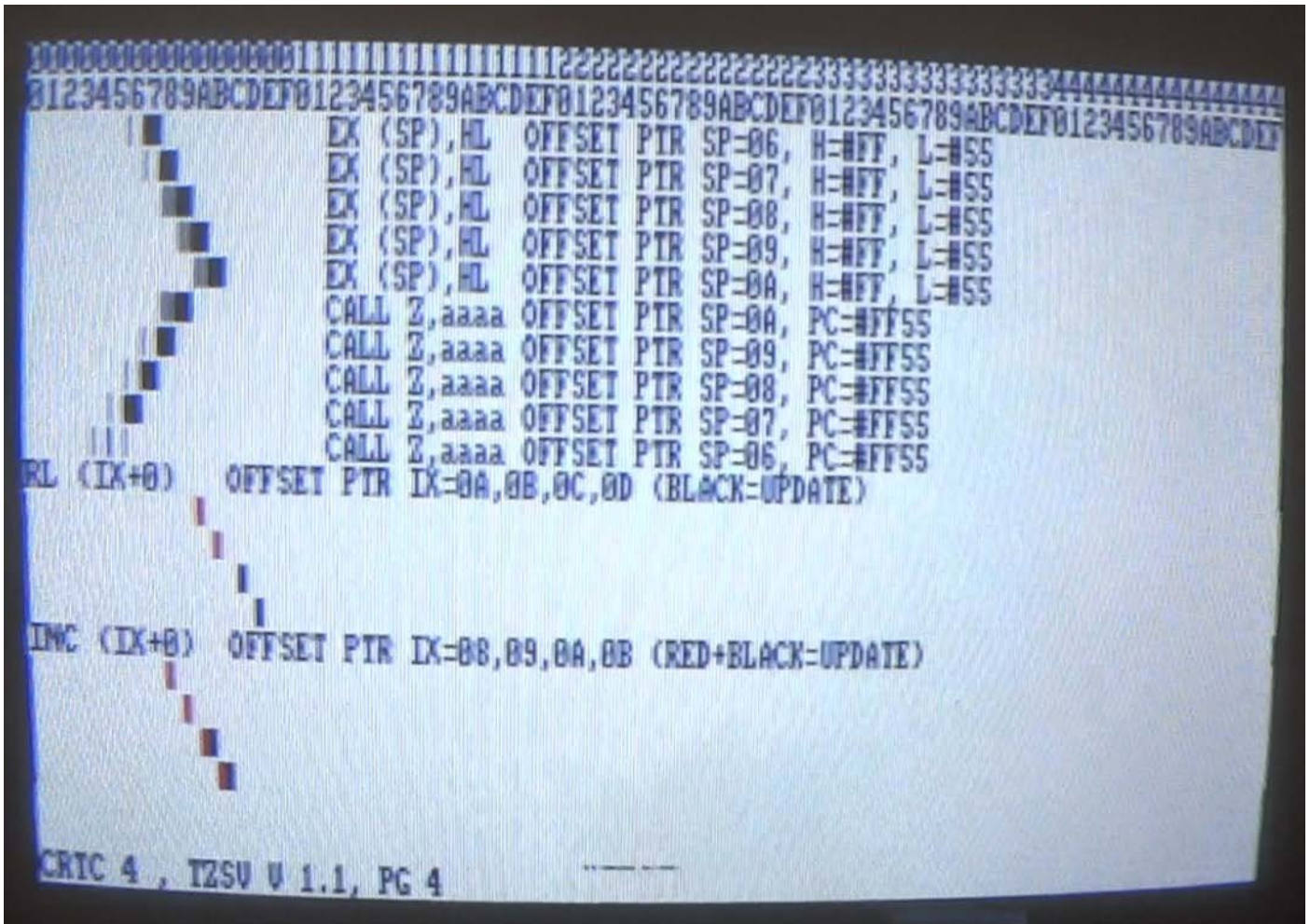
AMSTRAD CPC / CRTC 4 SHAKER V1.9 OUTPUT

LOGON SYSTEM 2021 / LONGSHOT

More information about CRTC in Amstrad Cpc Crtc Compendium
("con de chat canadien")

Sommaire

UPDATE VRAM VS CRTC.....	3
SKEW DISP ON R0 RUPTURE	6
INTERRUPT DELAY FROM R2	9
UPDATE CRTC R0 TIMING.....	11
R13 UPDATE IN 4 USEC SCREENS (R0=3).....	12
R13 UPDATE IN 2 USEC SCREENS (R0=1).....	15
R13 UPDATE IN 1 USEC SCREENS (R0=0).....	18
GATE ARRAY PIXELISATION	21
GATE ARRAY INKERISATION	22
GATE ARRAY MODERISATION	24
HSYNC DELAY ON MODE UPDATE, R2 UPDATE/R3 LENGTH 2 to 0	25
R2 UPDATE DURING & AFTER HSYNC	27
R3 UPDATE DURING HSYNC	31
R4 & R9 CHECKING.....	36
VSYNC CONDITIONS	37
R1 STORIES	39
R6 STORIES	43
RVNI (NON INVISIBLE VERTICAL RUPTURE)	50
ANALYZER / FORCED STABILISATION ON R0=0.....	51
R5 SCANNER (for CRTC 1).....	54
R5 STORIES / INTERACTIVE TEST.....	55
OFFSET UPDATE	56
« RVMB ».....	58
BOUNGA : CRTC 2 R4=R9=0 FORCED	71
INTERLACE VM	72
INTERLACE C4/C9 COUNTERS	74
INTERLACE CRTC 2 C9 STRANGER THING.....	86
FAKE VSYNC ON CRTC 2	87
CRTC 2 FIND C0 MIN.....	88
CRTC 2 - 1 LINE RUPTURE.....	89
CRTC 1 – BUG OUTI R0	90
CRTC 1- BE00 CHECK	92



Note : WinApe 2.0 Beta 3 wrong on LDI (page 3) and EX(SP),HL (page 4) (Ok with others instructions)

INTERRUPT DELAY FROM R2

```
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2, LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) USYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT (<) CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC USYNC FROM PPI.PORTB.0=1 !!
```

```
DELAY BETWEEN HSYNC (C0=R2) AND INTERRUPTION (INT)
WHEN R3=0E, INTERRUPT OCCURS #10 uSEC AFTER C0=R2 (HFF=NO INT)
WHEN R3=0D, INTERRUPT OCCURS #0F uSEC AFTER C0=R2 (HFF=NO INT)
WHEN R3=0C, INTERRUPT OCCURS #0E uSEC AFTER C0=R2 (HFF=NO INT)
WHEN R3=0B, INTERRUPT OCCURS #0D uSEC AFTER C0=R2 (HFF=NO INT)
WHEN R3=0A, INTERRUPT OCCURS #0C uSEC AFTER C0=R2 (HFF=NO INT)
WHEN R3=09, INTERRUPT OCCURS #0B uSEC AFTER C0=R2 (HFF=NO INT)
WHEN R3=08, INTERRUPT OCCURS #0A uSEC AFTER C0=R2 (HFF=NO INT)
WHEN R3=07, INTERRUPT OCCURS #09 uSEC AFTER C0=R2 (HFF=NO INT)
WHEN R3=06, INTERRUPT OCCURS #08 uSEC AFTER C0=R2 (HFF=NO INT)
WHEN R3=05, INTERRUPT OCCURS #07 uSEC AFTER C0=R2 (HFF=NO INT)
WHEN R3=04, INTERRUPT OCCURS #06 uSEC AFTER C0=R2 (HFF=NO INT)
WHEN R3=03, INTERRUPT OCCURS #05 uSEC AFTER C0=R2 (HFF=NO INT)
WHEN R3=02, INTERRUPT OCCURS #04 uSEC AFTER C0=R2 (HFF=NO INT)
WHEN R3=01, INTERRUPT OCCURS #03 uSEC AFTER C0=R2 (HFF=NO INT)
WHEN R3=00, INTERRUPT OCCURS #12 uSEC AFTER C0=R2 (HFF=NO INT)

USYNC DURATION (6=#180 ON CRT 0,3,4)(8=#400 ALL CRT / n=#400 CRT 1,2)
R3 High=6 >> SIZE=#0180 uSEC
R3 High=0 >> SIZE=#0400 uSEC

DELAY OF 'CALL TO #38' ON INTERRUPTION IS 05 uSEC (RST#38=4 uSEC)

CRTC 4
```


DELAY BETWEEN HSYNC (C0=R2) AND INTERRUPTION (IM2)

WHEN R3=	INTERRUPT OCCURS	#	uSEC	AFTER	C0=R2	(#FF=NO	INT)
0E	INTERRUPT OCCURS	#10	uSEC	AFTER	C0=R2	(#FF=NO	INT)
0D	INTERRUPT OCCURS	#0F	uSEC	AFTER	C0=R2	(#FF=NO	INT)
0C	INTERRUPT OCCURS	#0E	uSEC	AFTER	C0=R2	(#FF=NO	INT)
0B	INTERRUPT OCCURS	#0D	uSEC	AFTER	C0=R2	(#FF=NO	INT)
0A	INTERRUPT OCCURS	#0C	uSEC	AFTER	C0=R2	(#FF=NO	INT)
09	INTERRUPT OCCURS	#0B	uSEC	AFTER	C0=R2	(#FF=NO	INT)
08	INTERRUPT OCCURS	#0A	uSEC	AFTER	C0=R2	(#FF=NO	INT)
07	INTERRUPT OCCURS	#09	uSEC	AFTER	C0=R2	(#FF=NO	INT)
06	INTERRUPT OCCURS	#08	uSEC	AFTER	C0=R2	(#FF=NO	INT)
05	INTERRUPT OCCURS	#07	uSEC	AFTER	C0=R2	(#FF=NO	INT)
04	INTERRUPT OCCURS	#06	uSEC	AFTER	C0=R2	(#FF=NO	INT)
03	INTERRUPT OCCURS	#05	uSEC	AFTER	C0=R2	(#FF=NO	INT)
02	INTERRUPT OCCURS	#04	uSEC	AFTER	C0=R2	(#FF=NO	INT)
01	INTERRUPT OCCURS	#03	uSEC	AFTER	C0=R2	(#FF=NO	INT)
00	INTERRUPT OCCURS	#12	uSEC	AFTER	C0=R2	(#FF=NO	INT)

HSYNC DURATION (G=8180 ON CRT 0,3,4)(0=8400 ALL CRT / n=8400 CRT 1,2)

R3 High=0 >> SIZE=80180 uSEC

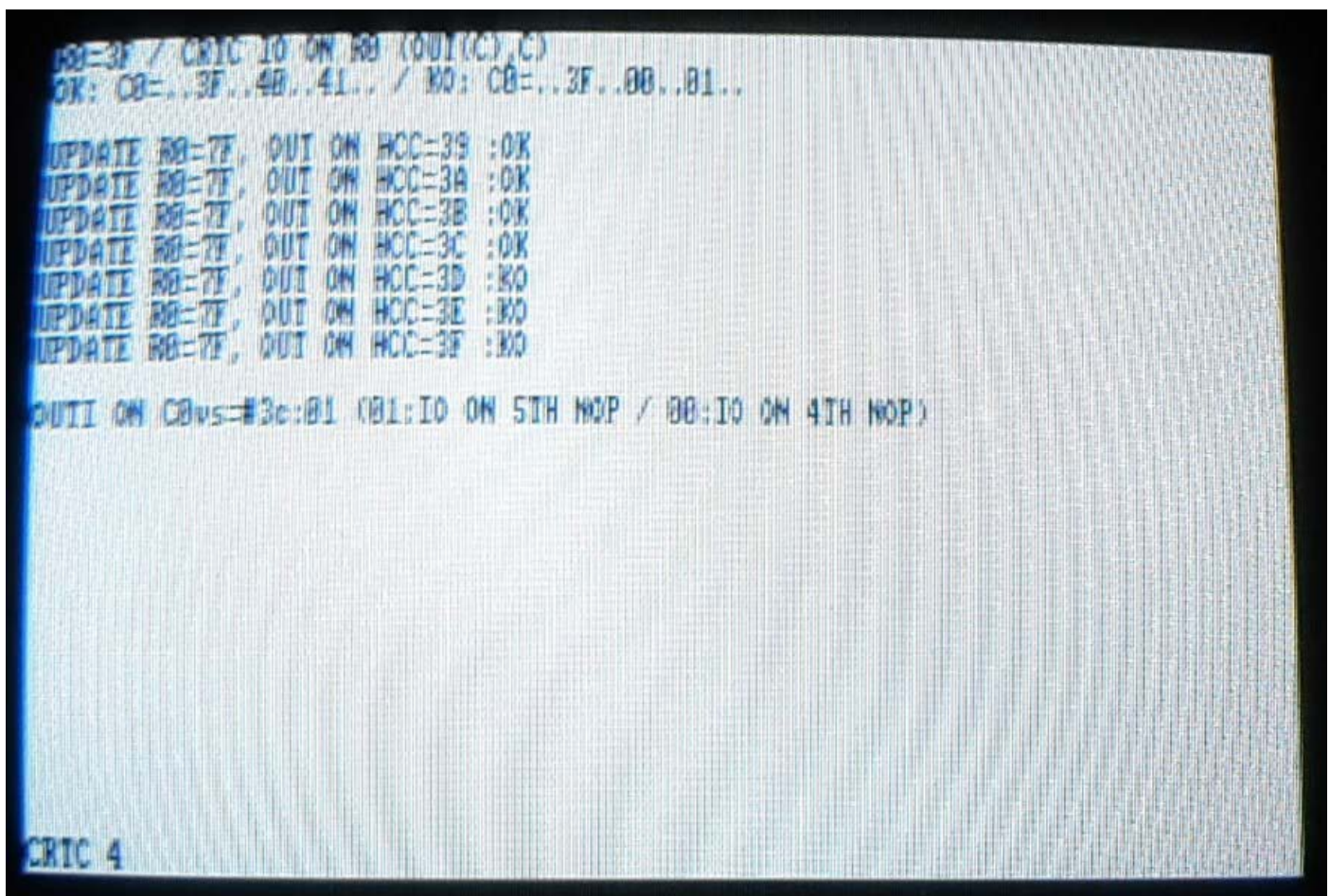
R3 High=0 >> SIZE=80400 uSEC

DELAY OF INTERRUPTION CALL (IM2) IS 07 uSEC

CRTC 4

UPDATE CRTC R0 TIMING

```
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE URAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2, LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) USYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUMI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT (<) CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC USYNC FROM PPI.PORTB.0=1 !!
```



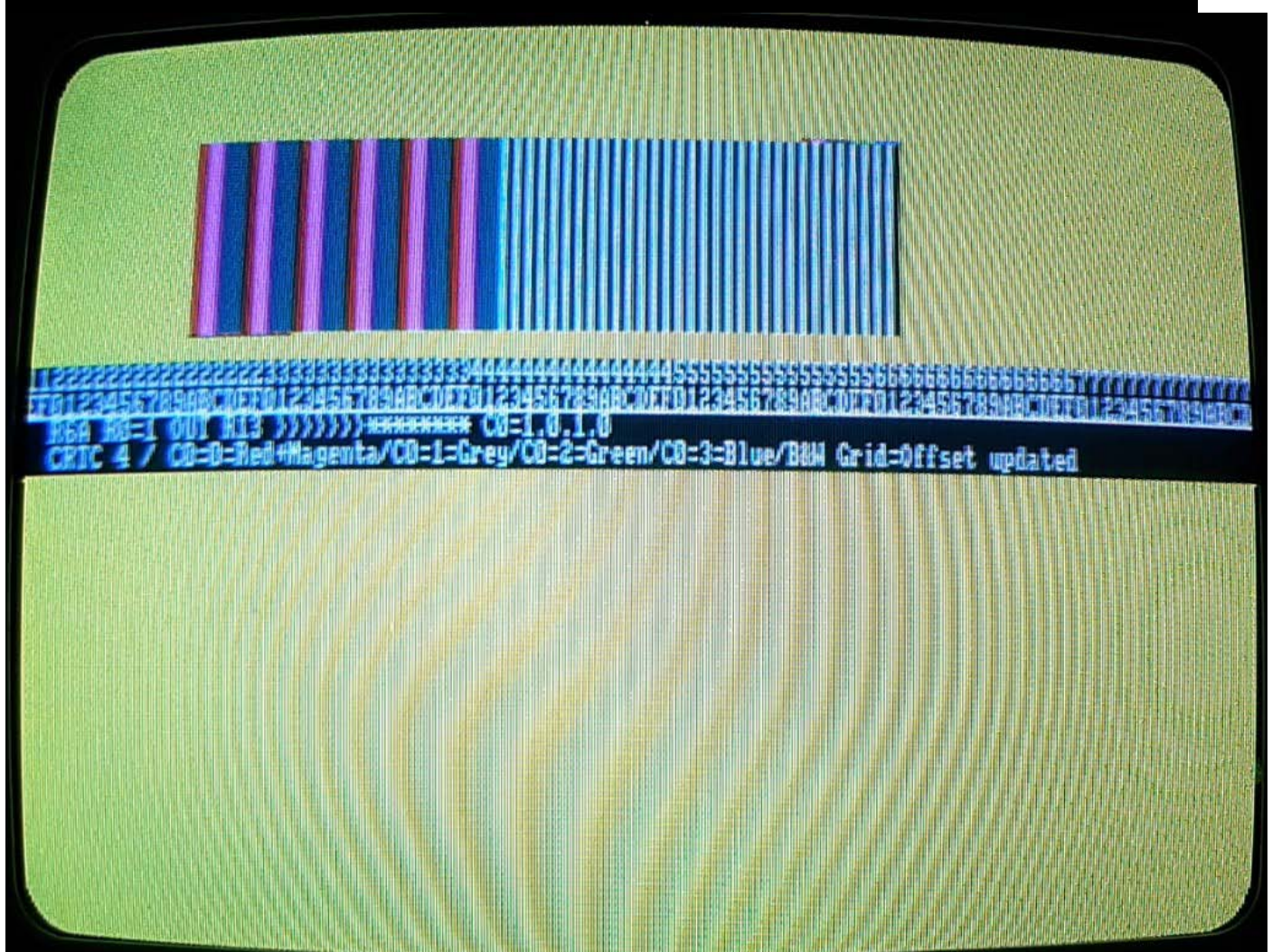
R13 UPDATE IN 4 USEC SCREENS (R0=3)

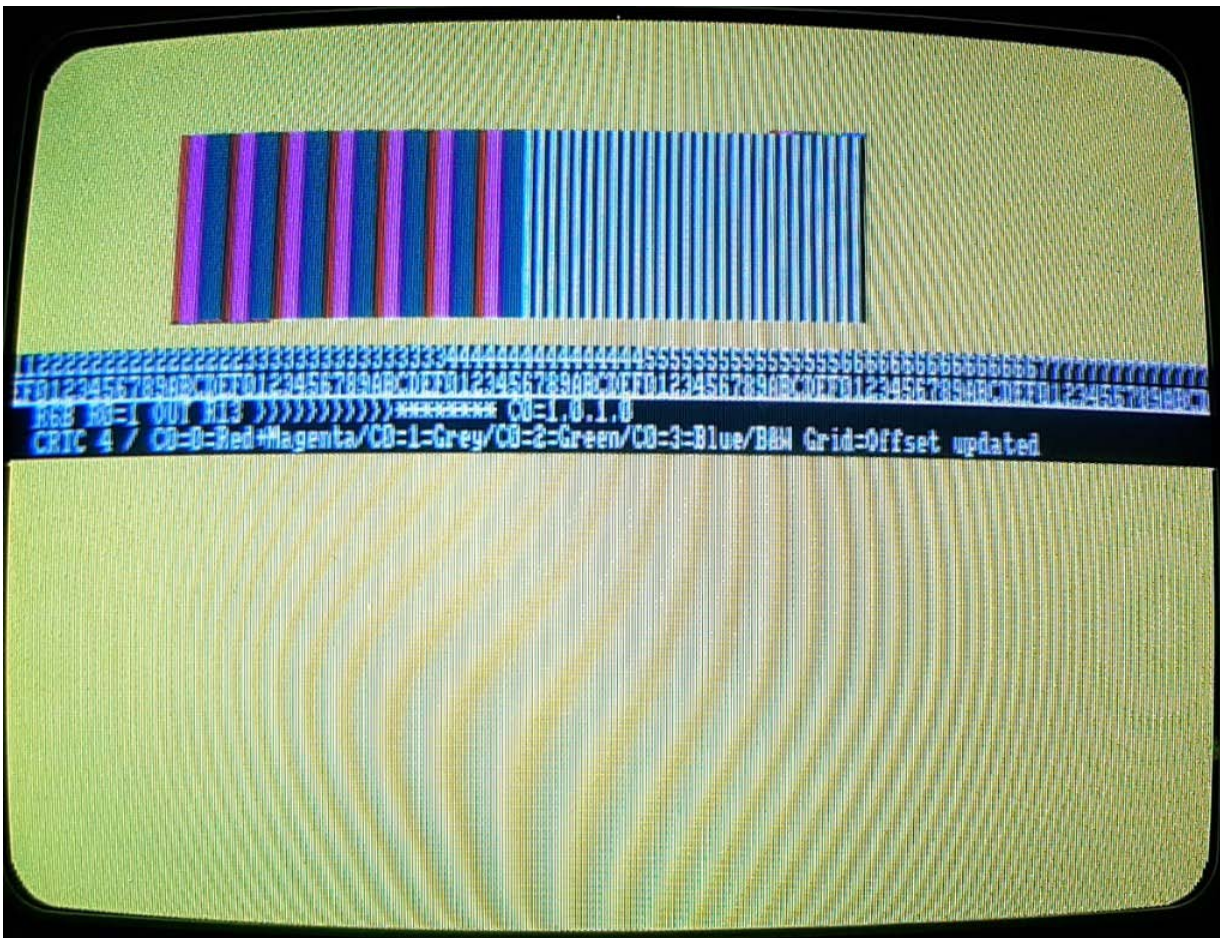
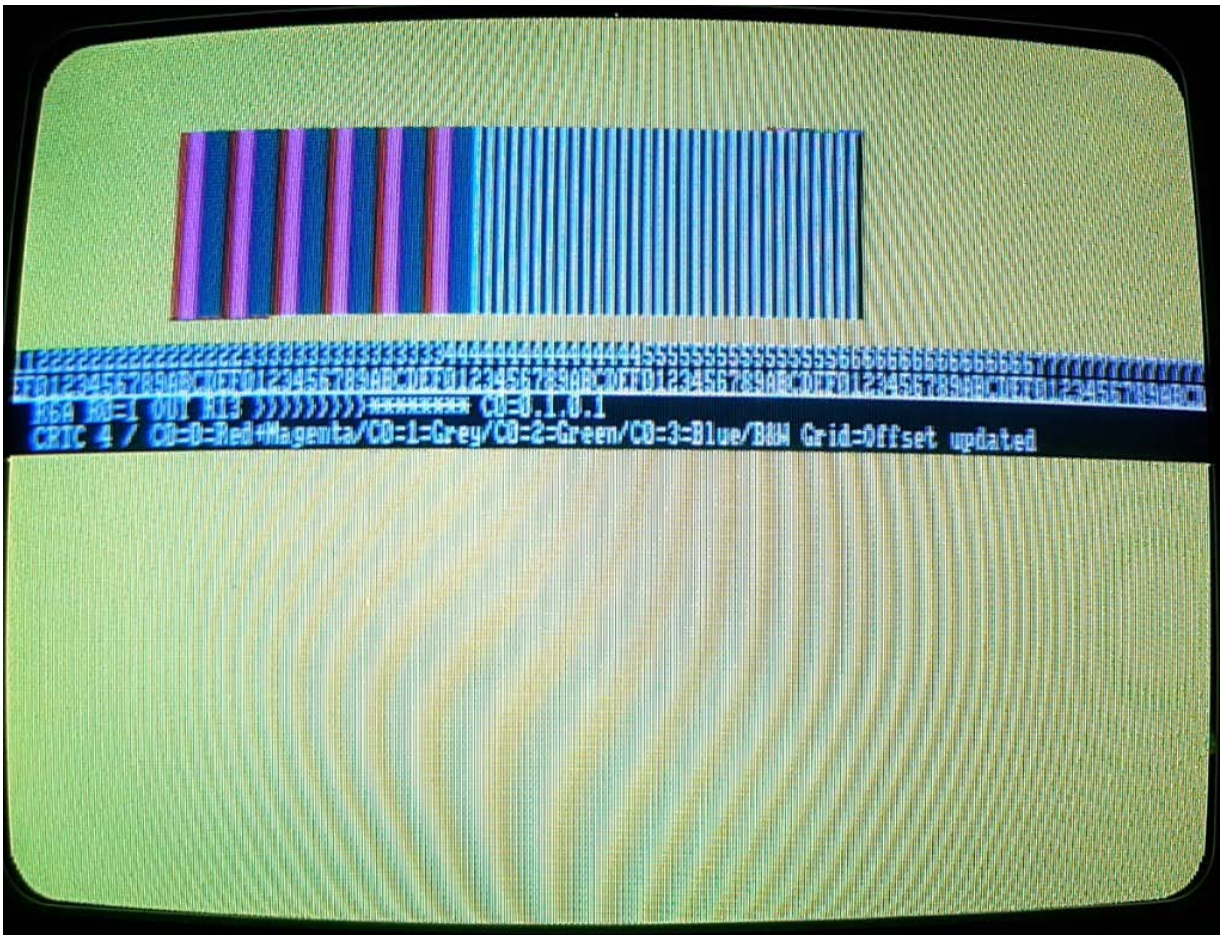
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CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE URAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2, LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUMI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT (<) CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
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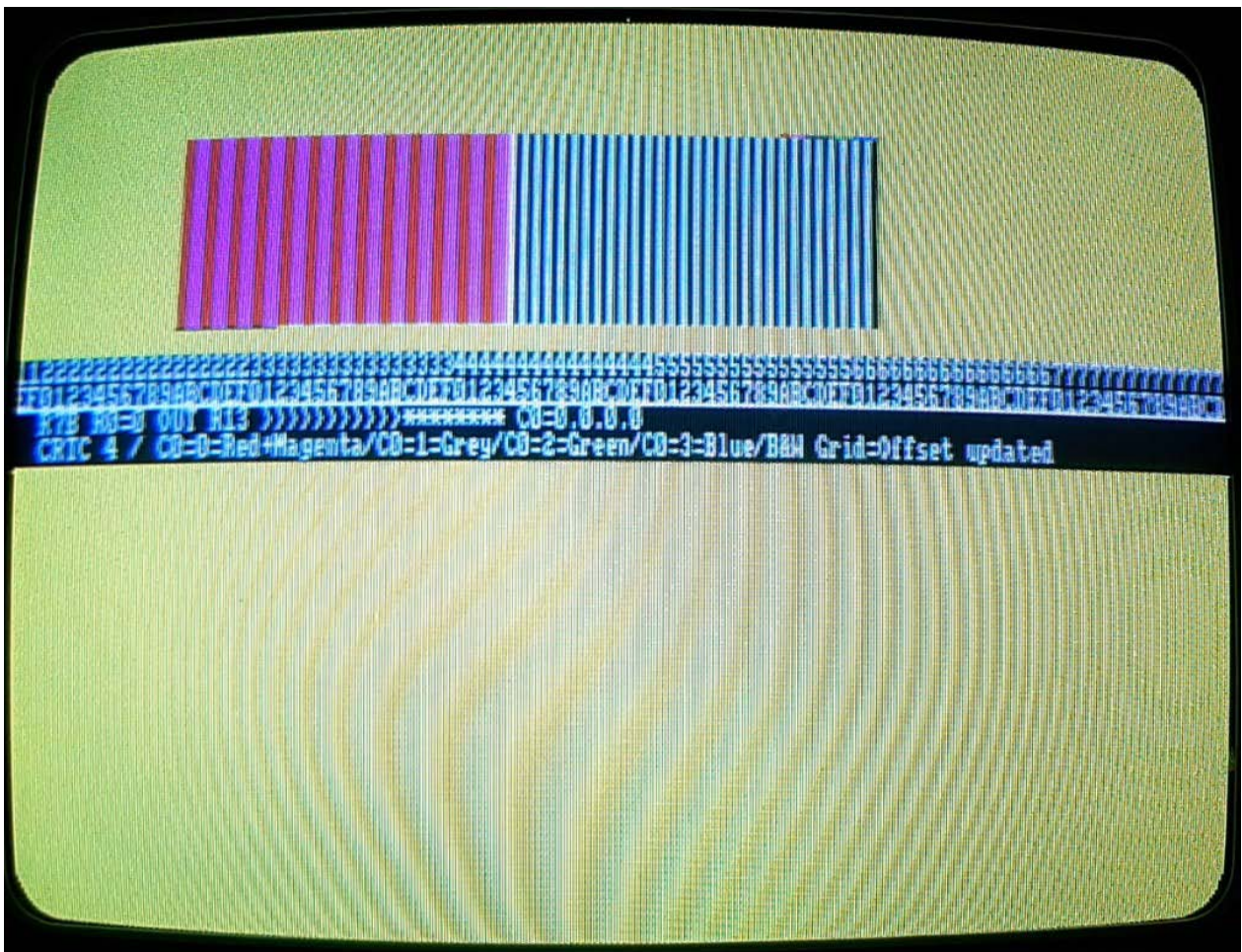
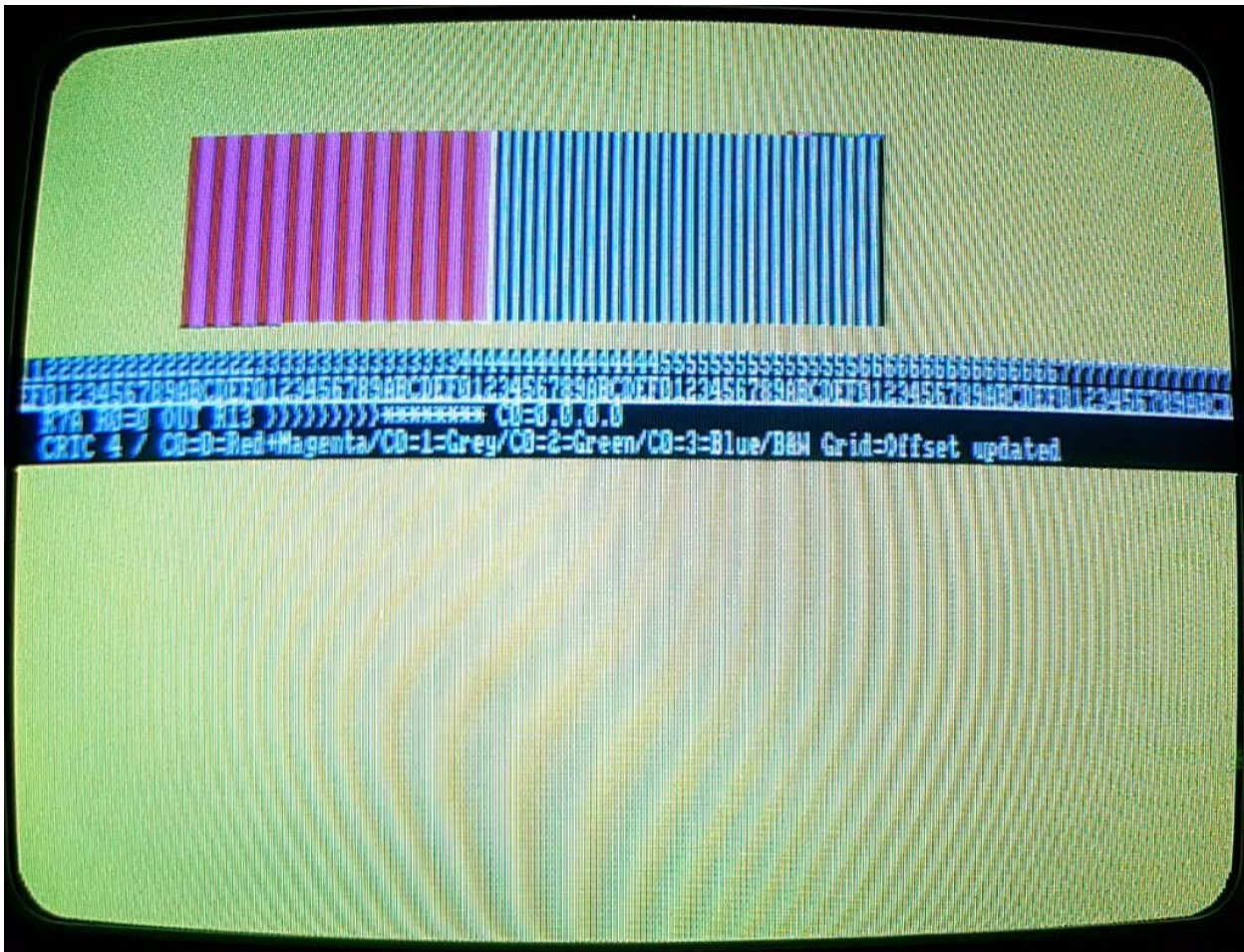


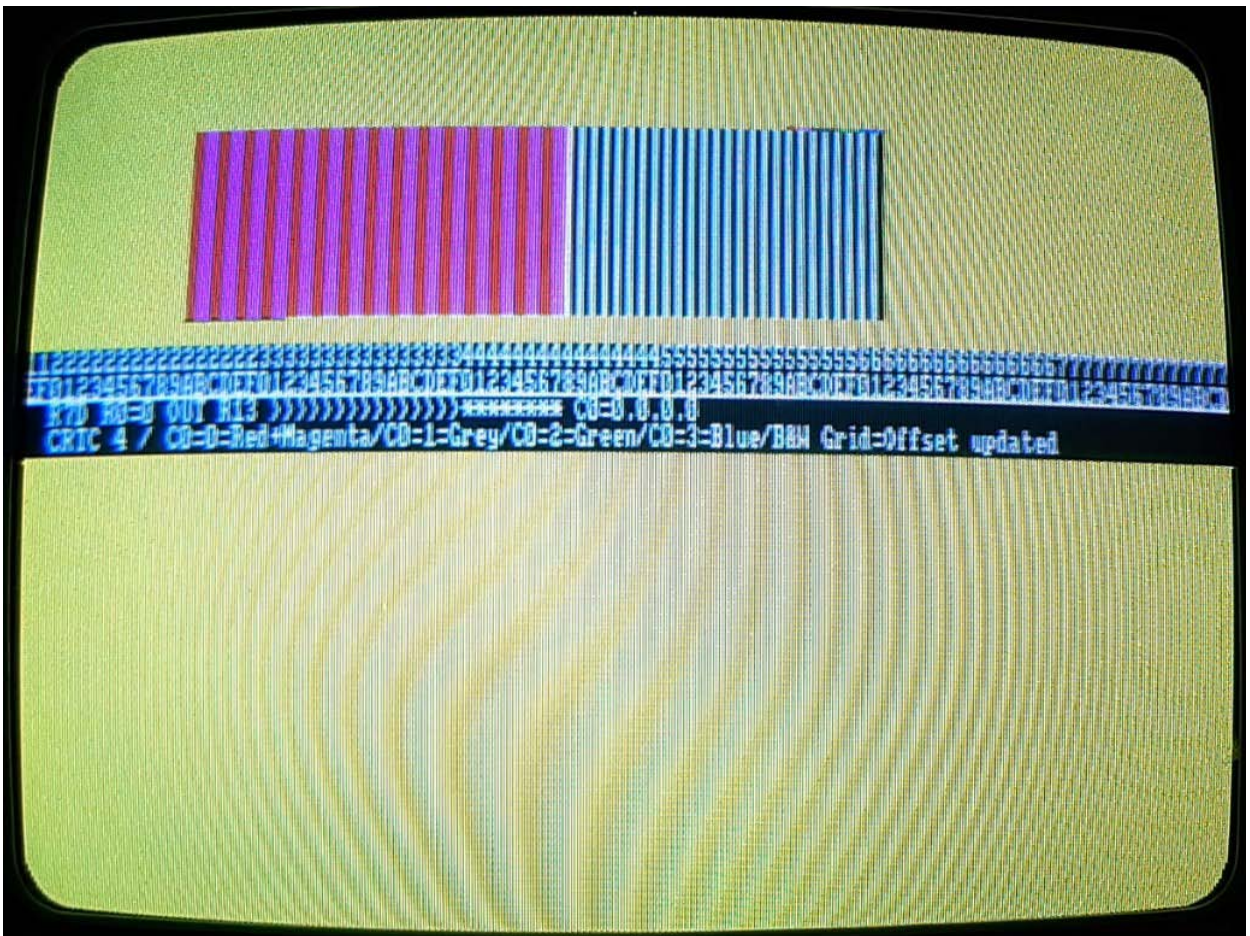
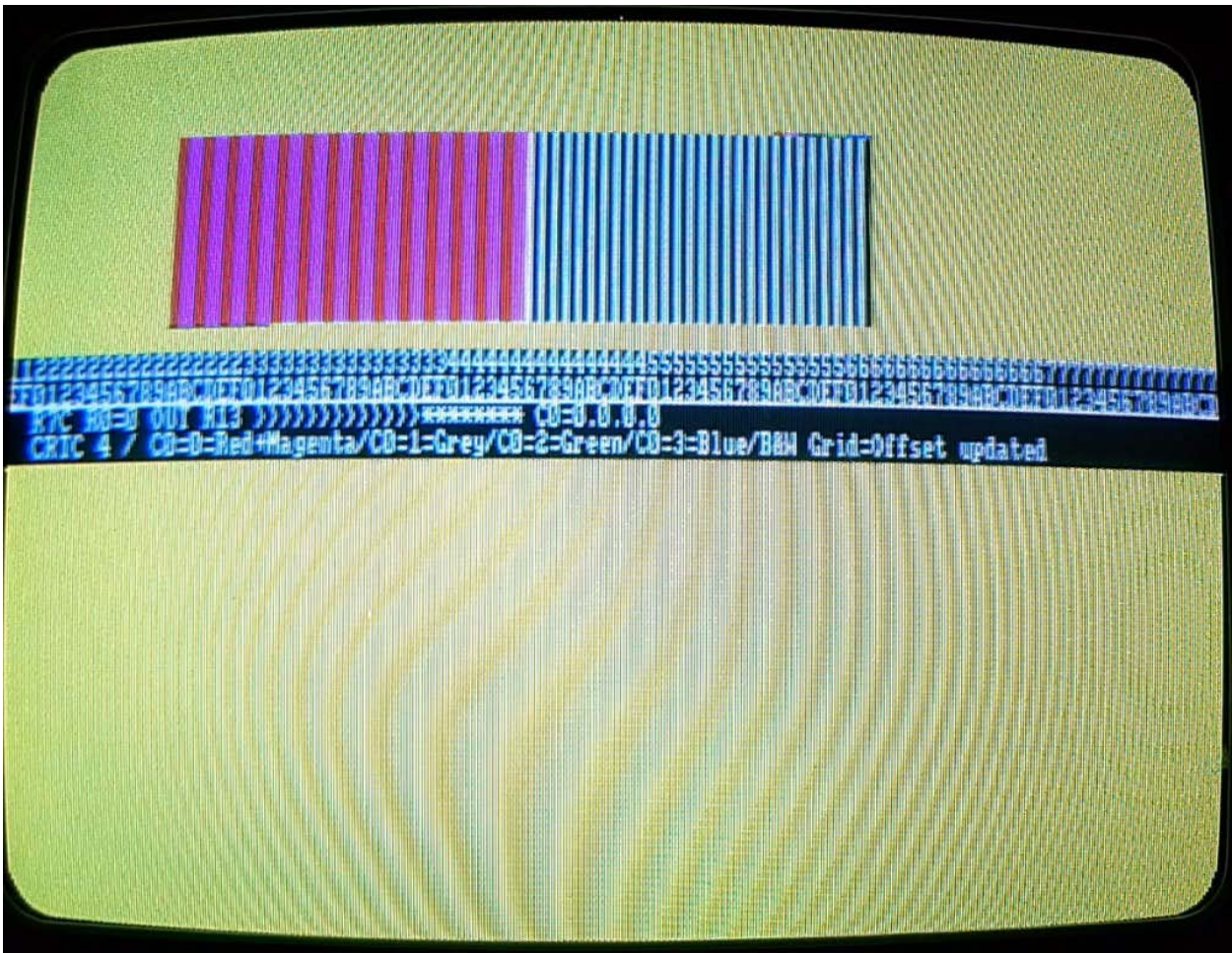
R13 UPDATE IN 2 USEC SCREENS (R0=1)

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CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE URAM VS CRTIC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTIC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2, LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUMI LTD
(CAPS) ANALYZER / FORCED STAB CRTIC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTIC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTIC CNT (<) CRTIC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTIC VSYNC FROM PPI.PORTB.0=1 !!
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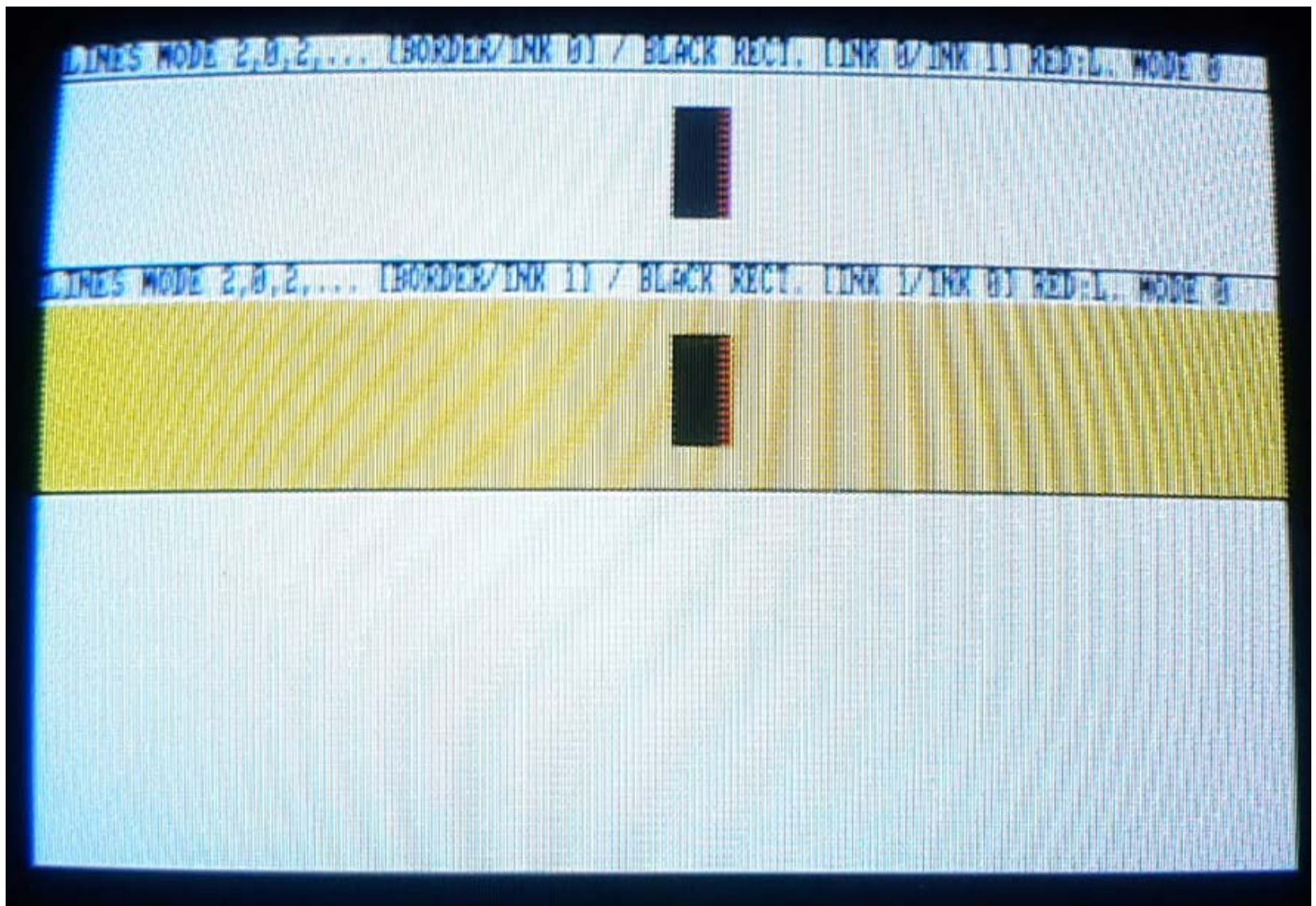






GATE ARRAY PIXELISATION

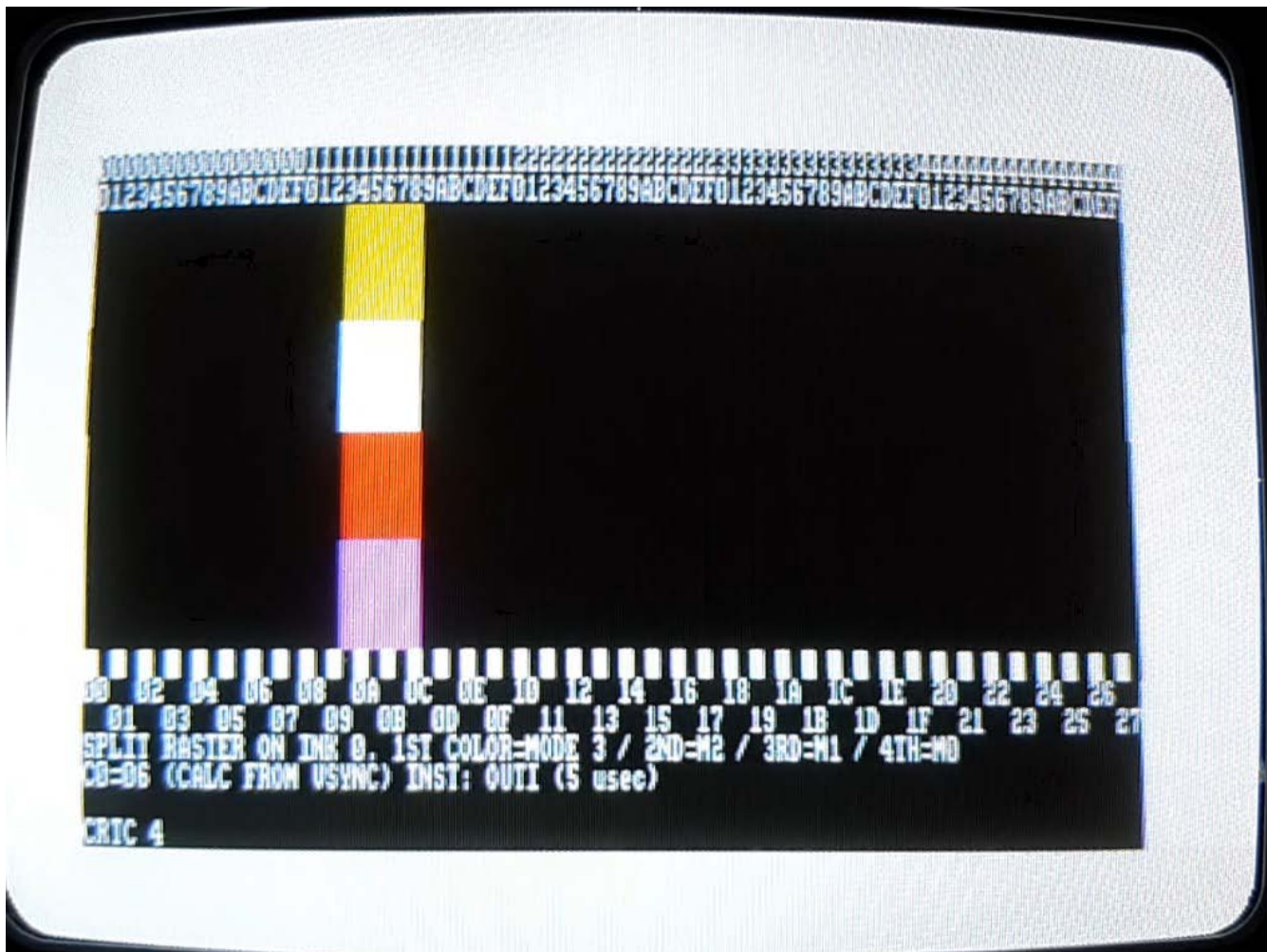
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CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2, LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```



GATE ARRAY INKERISATION

```

CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE URAM VS CRTIC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTIC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2, LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) USYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUMI LTD
(CAPS) ANALYZER / FORCED STAB CRTIC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTIC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTIC CNT (<) CRTIC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTIC USYNC FROM PPI.PORTB.0=1 !!
    
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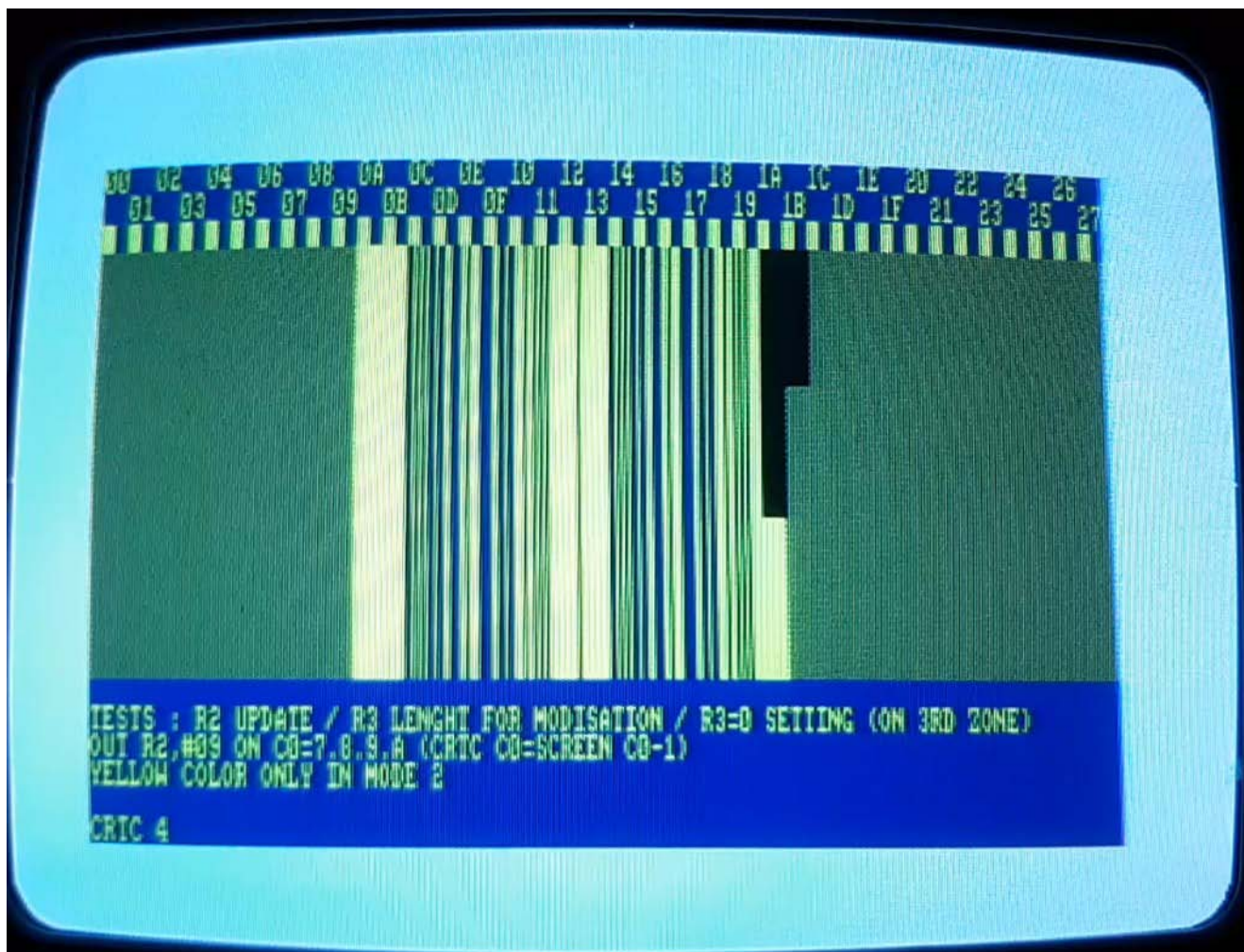
GATE ARRAY MODERISATION

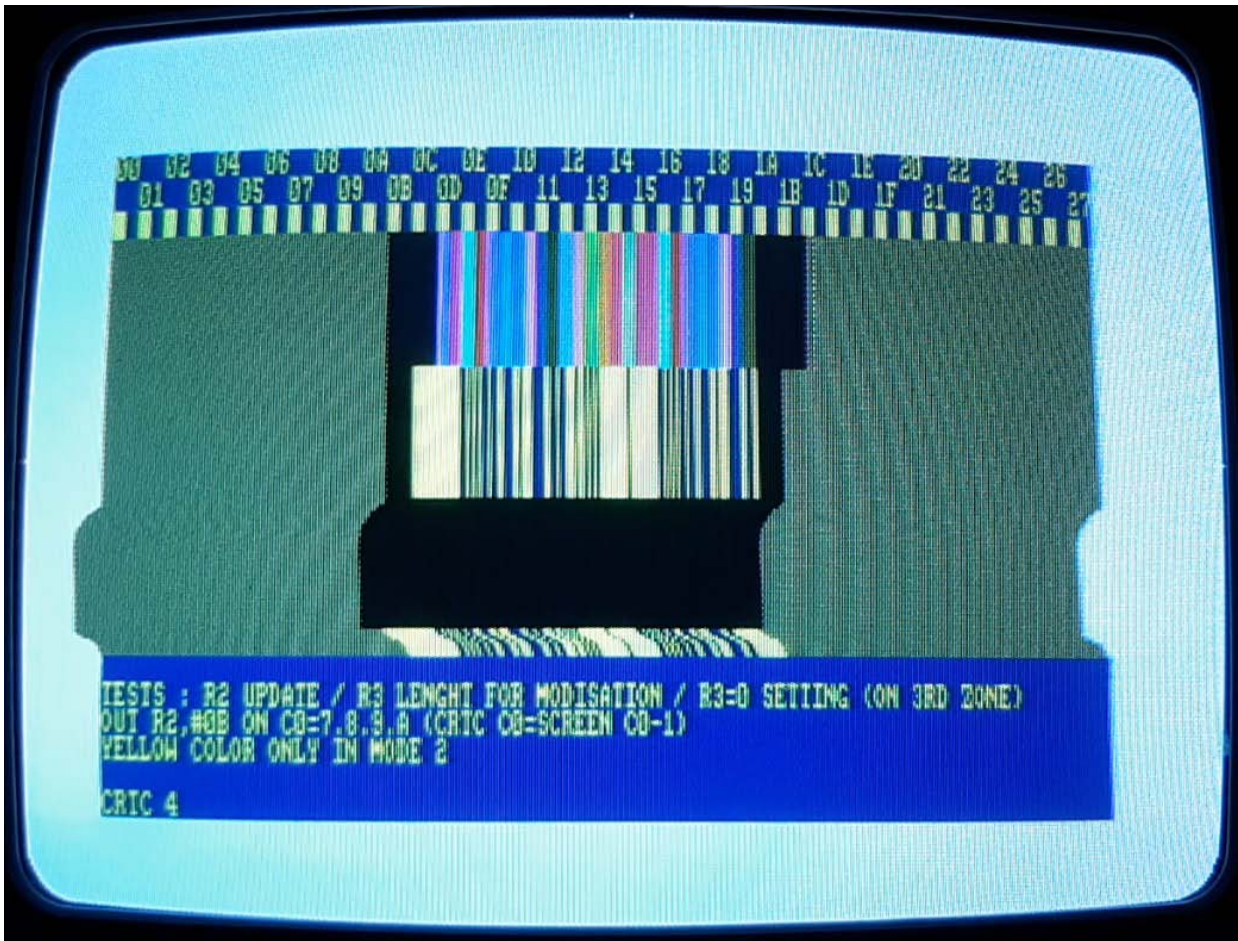
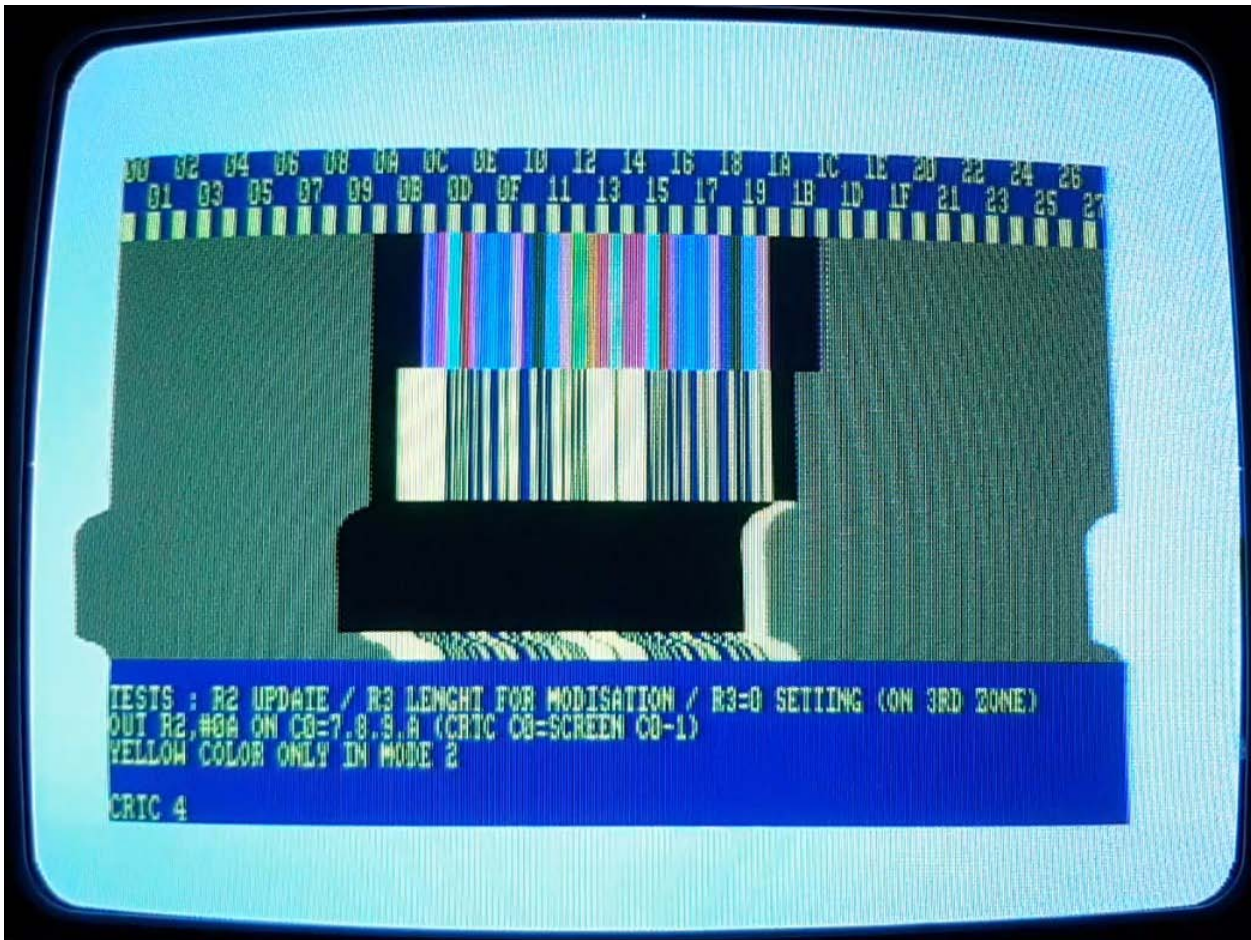
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CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE URAM VS CRTIC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTIC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
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(9) GATE ARRAY INKERISATION (3 TST)
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(R) HSYNC DELAY MODE UPD,UPD R2, LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUMI LTD
(CAPS) ANALYZER / FORCED STAB CRTIC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTIC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTIC CNT (<) CRTIC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTIC VSYNC FROM PPI.PORTB.0=1 !!
```



HSYNC DELAY ON MODE UPDATE, R2 UPDATE/R3 LENGTH 2 to 0

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE URAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
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(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2, LGTH R3 (2,1,0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) USYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUMI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT (<) CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC USYNC FROM PPI.PORTB.0=1 !!
```





R2 UPDATE DURING & AFTER HSYNC

```

CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE URAM VS CRTIC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTIC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2, LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) USYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUMI LTD
(CAPS) ANALYZER / FORCED STAB CRTIC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTIC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTIC CNT (<) CRTIC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTIC USYNC FROM PPI.PORTB.0=1 !!
    
```



R2 UPDATE DURING HSYNC

R2=#0B / R3=1B / CM CB=#0D0E0F10, OUT R2,#12 (+ R2=#2E ON CB=#23)

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26

CRTC 4

R2 UPDATE DURING HSYNC

R2=#0B / R3=1B / CM CB=#0D0E0F10, OUT R2,#13 (+ R2=#2E ON CB=#23)

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26

CRTC 4

R2 UPDATE DURING HSYNC

R2=#0B / R3=1B / ON C0=#0D0E0F10, OUT R2,#14 (+ R2=#2E ON C0=#23)

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26

CRTC 4

R2 UPDATE DURING HSYNC

R2=#0B / R3=1B / ON C0=#0D0E0F10, OUT R2,#15 (+ R2=#2E ON C0=#23)

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

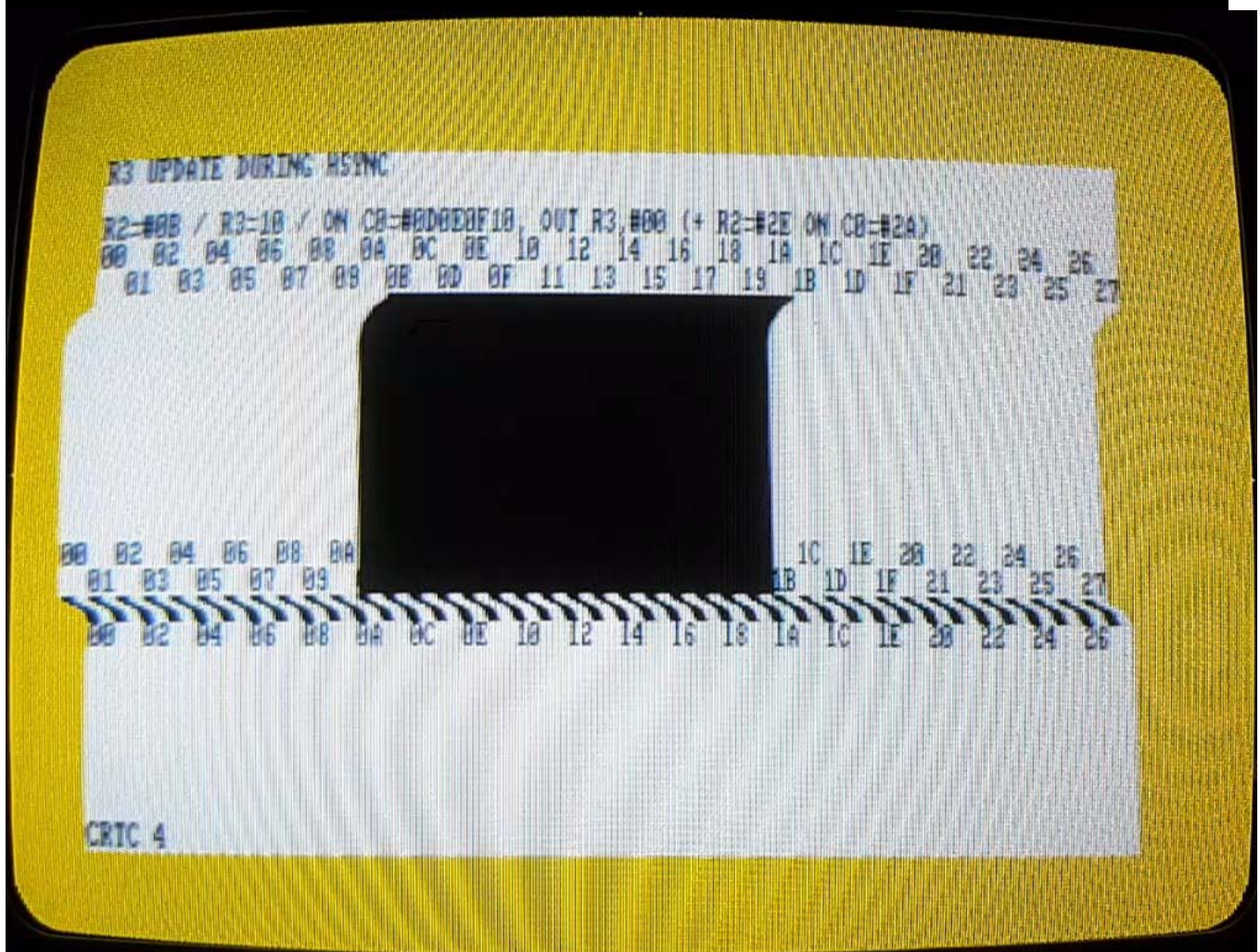
00 02 04 06 08 0A 26
01 03 05 07 09 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26

CRTC 4



R3 UPDATE DURING HSYNC

```
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE URAM VS CRTIC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTIC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD UPD R2, LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) USYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUMI LTD
(CAPS) ANALYZER / FORCED STAB CRTIC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTIC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTIC CNT (<) CRTIC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTIC USYNC FROM PPI.PORTB.0=1 !!
```



R3 UPDATE DURING HSYNC

R2=#0B / R3=1B / ON CB=#0D0E0F10, OUT R3,#01 (+ R2=#2E ON CB=#2A)

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 1C 1E 20 22 24 26
01 03 05 07 09 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26

CRTC 4

R3 UPDATE DURING HSYNC

R2=#0B / R3=1B / ON CB=#0D0E0F10, OUT R3,#02 (+ R2=#2E ON CB=#2A)

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 1E 20 22 24 26
01 03 05 07 09 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26

CRTC 4

R3 UPDATE DURING HSYNC

R2=#0B / R3=1B / CM CB=#0D0E0F1B, OUT R3,#03 (+ R2=#2E ON CB=#2A)

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A
01 03 05 07 09

1E 20 22 24 26
1F 21 23 25 27

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26

CRTC 4

R3 UPDATE DURING HSYNC

R2=#0B / R3=1B / CM CB=#0D0E0F1B, OUT R3,#04 (+ R2=#2E ON CB=#2A)

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A
01 03 05 07 09

20 22 24 26
1F 21 23 25 27

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26

CRTC 4

R3 UPDATE DURING HSYNC

R2=#0B / R3=1B / ON CB=#0D0E0F1B, OUT R3,#05 (+ R2=#2E ON CB=#2A)

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 11 13 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26

CRTC 4

R3 UPDATE DURING HSYNC

R2=#0B / R3=1B / ON CB=#0D0E0F1B, OUT R3,#06 (+ R2=#2E ON CB=#2A)

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 11 13 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26

CRTC 4

R3 UPDATE DURING HSYNC

R2=#0B / R3=10 / ON CB=#0D0E0F10, OUT R3,#07 (+ R2=#2E ON CB=#2A)

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

00 02 04 06 08 0A 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 13 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26

CRTC 4

VSYNC CONDITIONS

```
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE URAM VS CRTIC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTIC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2, LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUMI LTD
(CAPS) ANALYZER / FORCED STAB CRTIC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTIC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTIC CNT (<) CRTIC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTIC VSYNC FROM PPI.PORTB.0=1 !!
```

```
VSYNC MANAGEMENT DURING R3
R3 APPLIED ON ALL VALUES OF C4
R2=50, R3=12, R0=63 : V1=#5E, V2=#5F
R2=50, R3=13, R0=63 : V1=#5E, V2=#5F
R2=50, R3=14, R0=63 : V1=#5E, V2=#6F
R2=50, R3=15, R0=63 : V1=#5E, V2=#5F

R3 APPLIED ON ALL VALUES OF C4, EXCEPTED WHEN C4=R7 (C9=0) (THEN R3=12)
R2=50, R3=12, R0=63 : V1=#5E, V2=#5F
R2=50, R3=13, R0=63 : V1=#5E, V2=#5F
R2=50, R3=14, R0=63 : V1=#5E, V2=#5F
R2=50, R3=15, R0=63 : V1=#5E, V2=#5F
R2=50, R3=15, R0=63 : V1=#5E, V2=#5F ON PREVIOUS LINE
VSYNC CONDITIONS IN HSYNC (R2=#2E/R3=14)
>> UPD R7=C4 ON C9=0, C0v=#35 PPI.B ON C9=0, C0v=#3A:#5E
>> UPD R7=C4 ON C9=0, C0v=#35 PPI.B ON C9=0, C0v=#3E:#5E
>> UPD R7=C4 ON C9=0, C0v=#35 PPI.B ON C9=1, C0v=#3A:#5E
>> UPD R7=C4 ON C9=0, C0v=#35 PPI.B ON C9=1, C0v=#3E:#5E

PPI.STATUS Sus BEFORE R7=C4 :#5E
PPI.STATUS Sus AFTER UPD R7(<)C4 (R7=C4 BEFORE)(VSYNC CANCEL)(C9=0):#5E
PPI.ST C0=46 15 LINES AFTER R7=C4 ON C0vsio=#1E:5E,5E,5E,5E,5E,5E

CRTIC 4
```


R1 STORIES

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTIC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTIC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2, LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) USYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUMI LTD
(CAPS) ANALYZER / FORCED STAB CRTIC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTIC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTIC CNT (<) CRTIC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTIC USYNC FROM PPI.PORTB.0=1 !!
```

```
CRTC 4 R1 STORIES
STORY 1 : UPDATE VMA/VMA' CONDITIONS - DISPEN OFF/ON COND.
PROCESS : UPDATE R1 ON 16 LINES FROM L1 (R1=40-n, n=1..16)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
(L1)AT #C000+(5x80)
(L2)AT #C000+(6x80)
(L3)AT #C000+(7x80)
```


CRTC 4 R1 STORIES

STORY 2 : R1 > R0 WHEN C9=R9 & C9<R9

PROCESS : UPDATE R1 ON 16 LINES (64 x 7, 40 (C9=7))+(40 x 7, 64(C9=7))

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26

01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

(L1)AT #C000+(5x00)

(L2)AT #C000+(6x00)

(L2)AT #C000+(6x00)

(L3)AT #C000+(7x00)

CRTC 4 R1 STORIES

STORY 3 : R1=0 EFFECT (EACH LINE : 4 x OUT R1,0/OUT R1,40)

PROCESS : UPDATE R1=0 FOR 4x8 Lines FROM C0=0C, C0=30, C0=3E, C0=3F

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26

01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

(L2)AT #C000+(6x00)

(L3)AT #C000+(7x00)

R6 STORIES

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE URAM VS CRTIC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTIC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2, LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUMI LTD
(CAPS) ANALYZER / FORCED STAB CRTIC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTIC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTIC CNT (<) CRTIC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTIC VSYNC FROM PPI.PORTB.0=1 !!
```


CRTC 4 R6 STORIES (3 RUPTURES ON SCREEN)
TBI-R6-B IN 5 SEC. (PRESS SPACE, OR WAIT 4 SEC IN AUTO MODE)

CRTC 4 R6 STORIES (3 RUPTURES ON SCREEN)
T82-58 L. PATCHWORK R6-B/B FROM VERY 1ST LINE OF MIDDLE SCREEN RUPT (C4-B, C9-B)

CRTC 4 R6 STORIES (3 RUPTURES ON SCREEN)
T83-58 L. PATCHWORK R6-B/B FROM 2ND LINE OF MIDDLE SCREEN RUPTURE (C4-B, C9-1)

CRTC 4 R6 STORIES (3 RUPTURES ON SCREEN)
TB4-1ST LINE IN DISPLAY AREA : SEQUENCE R6-B/R6-8/ WHEN R1/RB

CRTC 4 R6 STORIES (3 RUPTURES ON SCREEN)
TB5-5B L. FROM 2ND LINE IN DISP AREA : PATCHWORK R6-B/R6-8 WHEN R1/RB

CRIC 4 R6 STORIES -AGAIN-
T86A-ON C4=9/C3=0 PATCHWORK R6=9/25 IN DISP AREA FOR 64 LINES

CRIC 4 R6 STORIES -AGAIN-
T86B-ON C4=9/C3=1 PATCHWORK R6=9/25 IN DISP AREA FOR 64 LINES

CRTC 4 R6 STORIES -AGAIN-
R6=8/25 IN DISP AREA FOR 64 LINES

CRTC 4 R6 STORIES -LAST LINE-
R6=8/TF FROM C0=2 ON C4=R4, C9=8..7, PREVIOUS R6=R4+1

..7, PREVIOUS R6=R4+1

CRTC 4 R6 STORIES -LAST LINE-
R6=8/TF FROM C0=2 ON C4=R4, C9=8..7, PREVIOUS R6=R4+1

CRTC 4 R6 STORIES -LAST LINE-
R6=B/TF FROM CB=2 IN U.ADJ ZONE (R5=16) (C4=fnc(CRTC)) PREVIOUS R6=R4+3

(R5=16) (C4=fnc(CRTC)) PREVIOUS R6=R4+3

CRTC 4 R6 STORIES -LAST LINE-
R6=B/TF FROM CB=2 IN U.ADJ ZONE

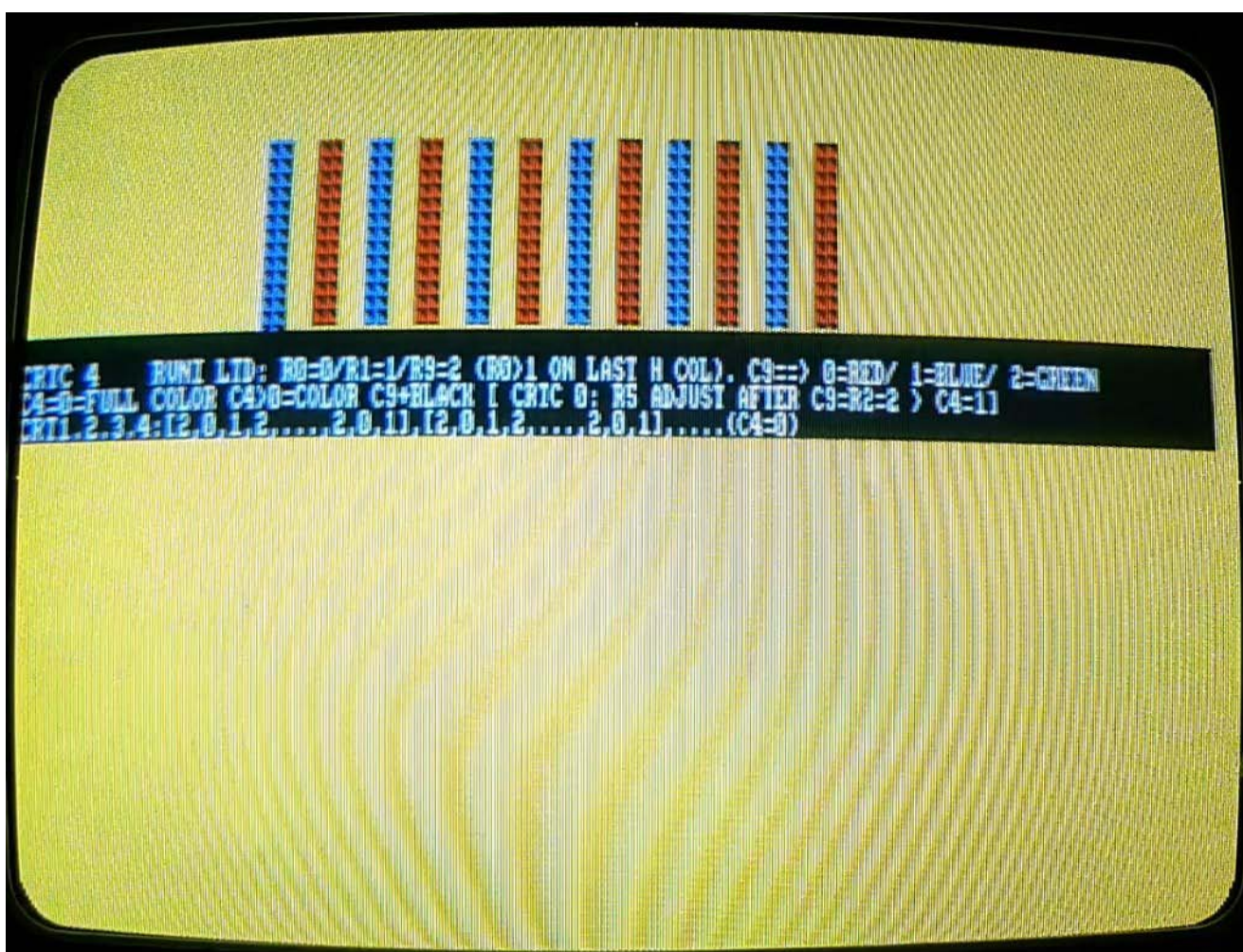
CRTC 4 R6 STORIES -LAST LINE-
R6=R4+1/TF FROM CB=2 IN U.ADJ ZONE (R5=16) (C4=fnc(CRTC)) PREVIOUS R6=R4+3

NE (R5=16) (C4=fnc(CRTC)) PREVIOUS R6=R4+3

CRTC 4 R6 STORIES -LAST LINE-
R6=R4+1/TF FROM CB=2 IN U.ADJ DO

RVNI (NON INVISIBLE VERTICAL RUPTURE)

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2, LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```



R5 SCANNER (for CRTC 1)

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE URAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2, LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUMI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT (<) CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
(O) CRTC 2 RUMB
(F0) BOUNGA:CRTC 2 ZERO!
(F1) INTERLACE VM (27 TST)
```

Only for CRTC 1

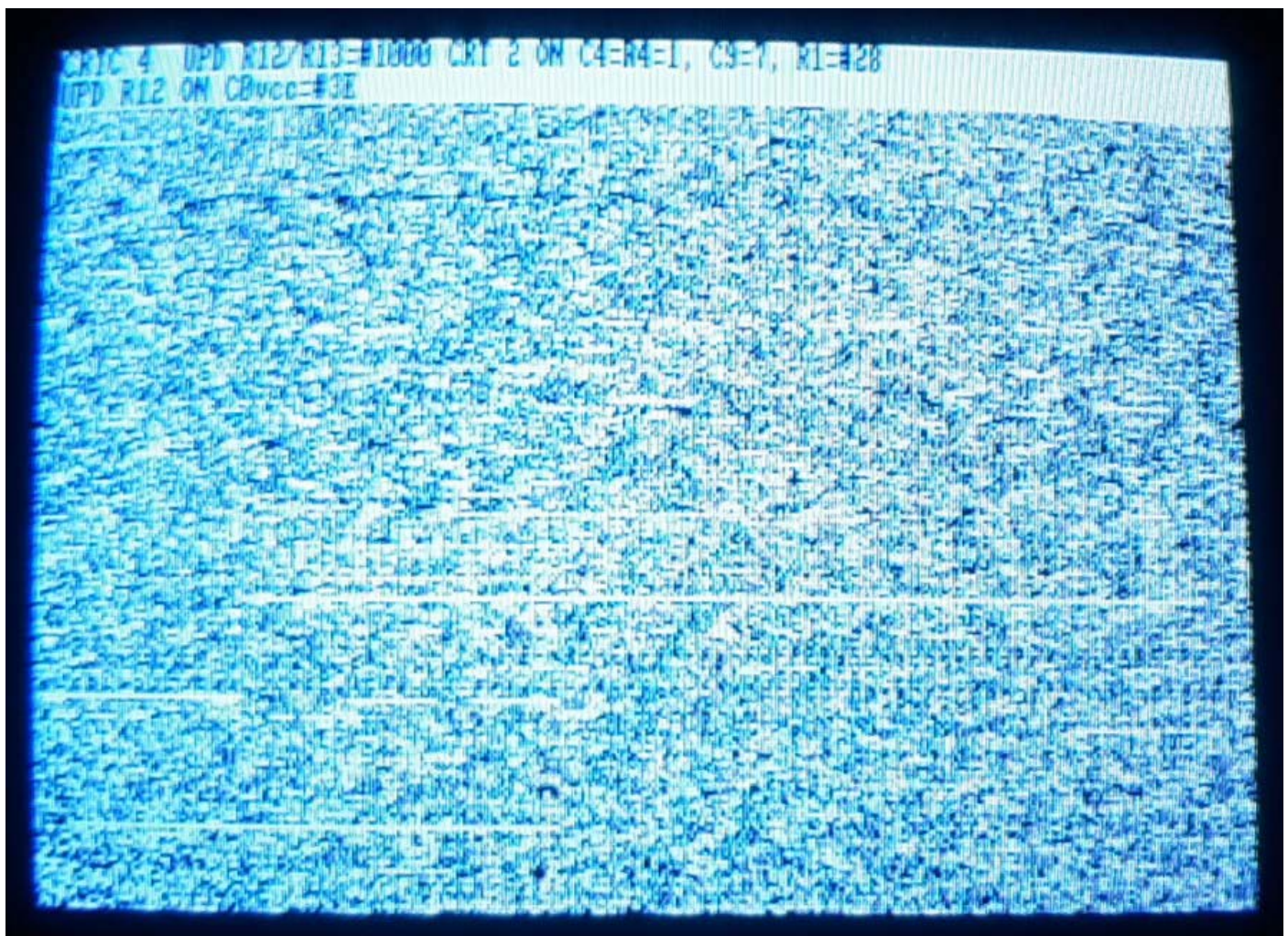
R5 STORIES / INTERACTIVE TEST

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE URAM VS CRTIC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTIC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2, LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUMI LTD
(CAPS) ANALYZER / FORCED STAB CRTIC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTIC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTIC CNT (<) CRTIC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTIC VSYNC FROM PPI.PORTB.0=1 !!
```

Only for CRTIC 1

OFFSET UPDATE

```
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE URAM VS CRTIC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTIC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2, LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUMI LTD
(CAPS) ANALYZER / FORCED STAB CRTIC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTIC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTIC CNT (<) CRTIC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTIC VSYNC FROM PPI.PORTB.0=1 !!
```



CRIC 4 UPD R12/R13=#1000 CRT 2 ON C4=R4=1, C9=7, R1=#28
UPD R12 ON CBVCC=#3F
CRIC 4 UPD R12/R13=#1000 CRT 2 ON C4=R4=1, C9=7, R1=#28
UPD R12 ON CBVCC=#3F

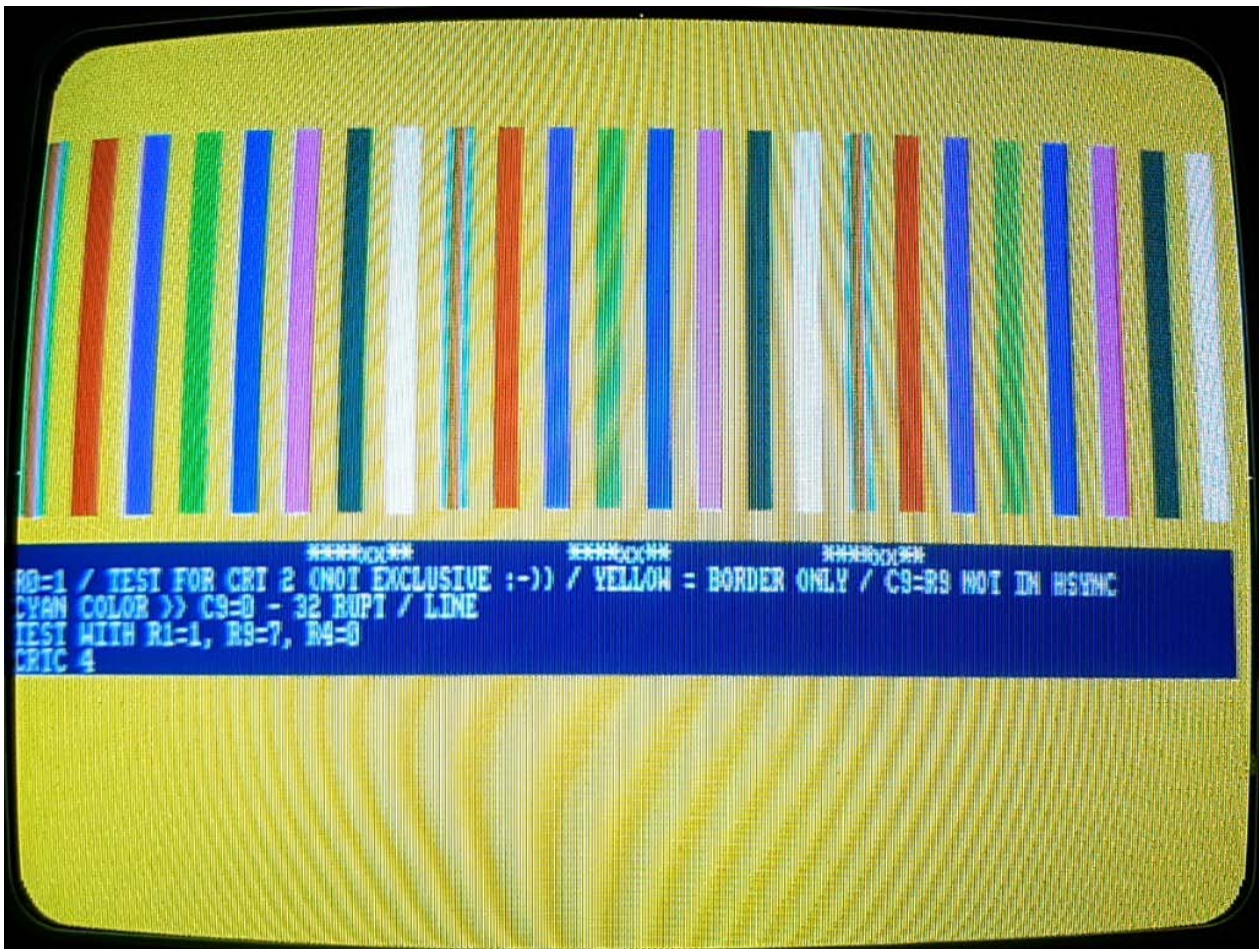
« RVMB »

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE URAM VS CRTIC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTIC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2, LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUMI LTD
(CAPS) ANALYZER / FORCED STAB CRTIC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTIC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTIC CNT <> CRTIC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTIC VSYNC FROM PPI.PORTB.0=1 !!

(O) CRTIC 2 RVMB
(F0) BOUNGA: CRTIC 2 ZERO!
(F1) INTERLACE VM (27 TST)
```







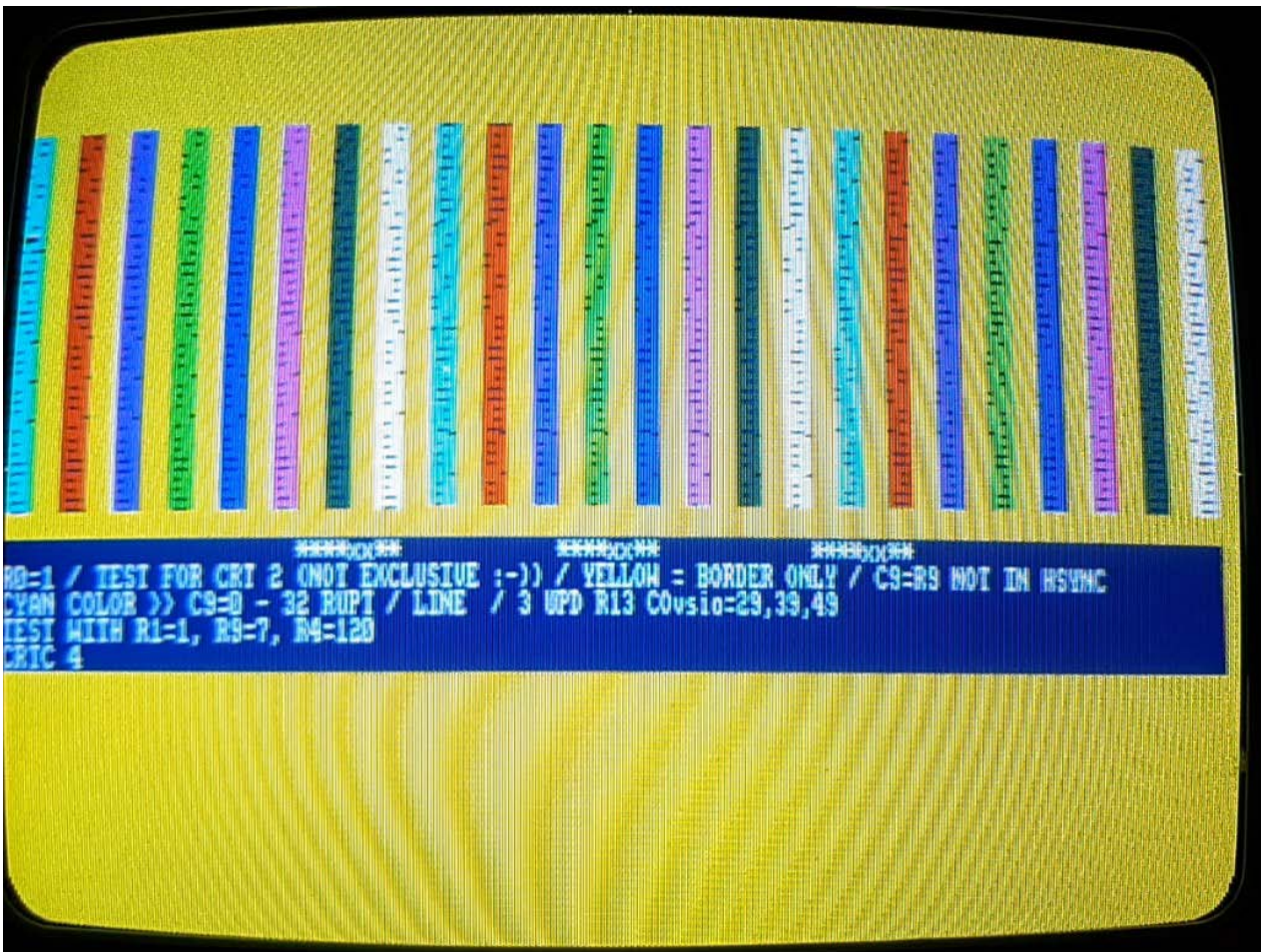












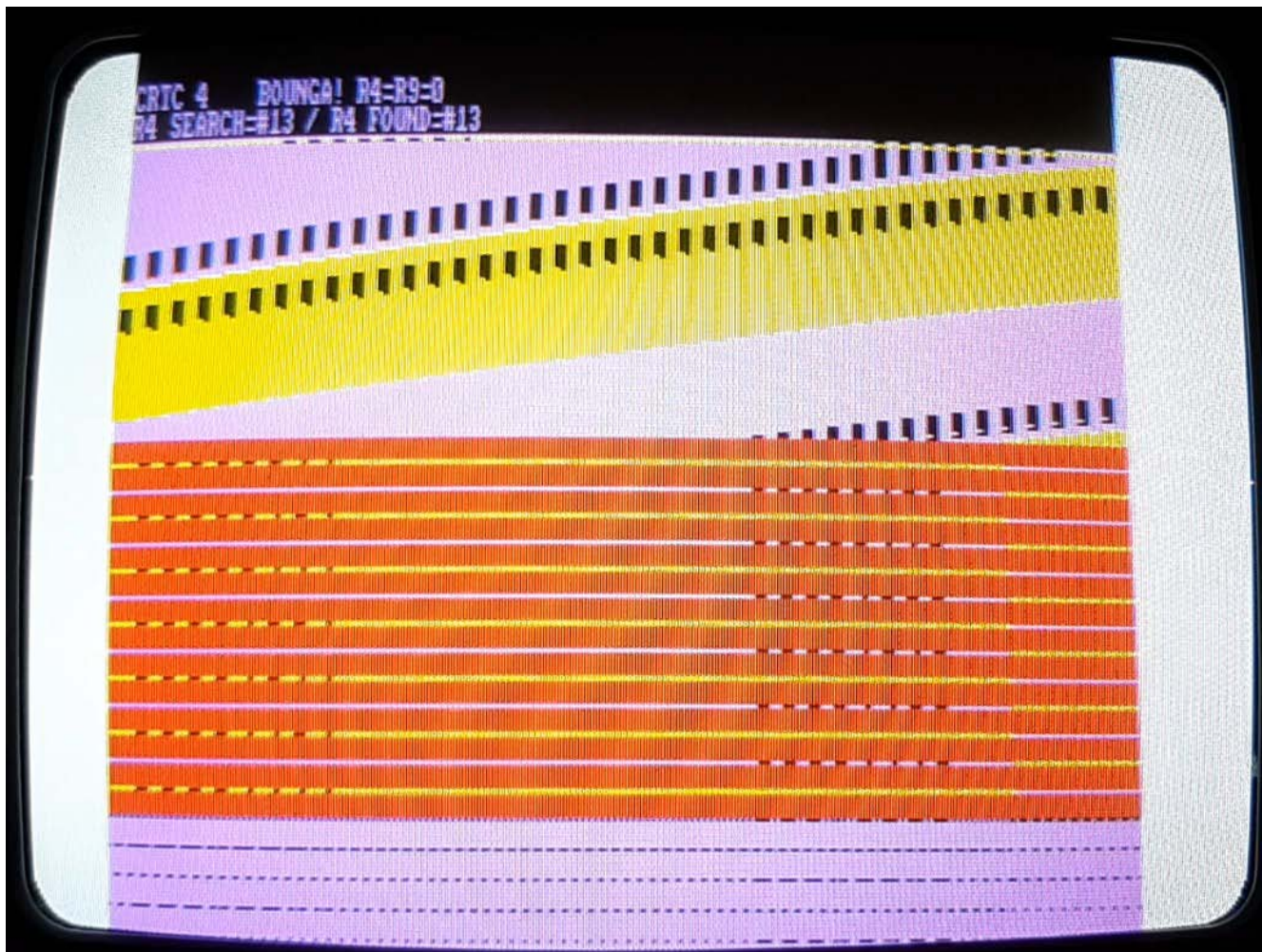




BOUNGA : CRTC 2 R4=R9=0 FORCED

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE URAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2, LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) USYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUMI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT (<) CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC USYNC FROM PPI.PORTB.0=1 !!
```

```
(0) CRTC 2 RUMB
(F0) BOUNGA:CRTC 2 ZERO!
(F1) INTERLACE VM (27 TST)
```



INTERLACE VM

```
CPC SHAKER 1.8 / LONGSHOT, LOGON SYSTEM
(1) UPDATE URAM VS CRTIC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTIC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2, LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) USYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUMI LTD
(CAPS) ANALYZER / FORCED STAB CRTIC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTIC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTIC CNT (<) CRTIC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTIC USYNC FROM PPI.PORTB.0=1 !!

(O) CRTIC 2 RUMB
(F0) BOUNGA: CRTIC 2 ZERO!
(F1) INTERLACE VM (27 TST)
```

```
CRTIC 4 INTERLACE VIDEO MODE
CALC WITH R6=#19:
R8=3 ON LINE 0 : FRAME SIZE=#2C00 usec (R9=7)(R7=0)
R8=3 ON LINE 1 : FRAME SIZE=#2C20 usec (R9=7)(R7=0)
R8=3 ON LINE 2 : FRAME SIZE=#2C40 usec (R9=7)(R7=0)
R8=3 ON LINE 3 : FRAME SIZE=#2C60 usec (R9=7)(R7=0)
R8=3 ON LINE 4 : FRAME SIZE=#2C80 usec (R9=7)(R7=0)
R8=3 ON RASTER LINE 2 / R0=0 ON LINE 43 / FRAME SIZE=#4600 usec (R9=7)(R7=0)
CALC WITH R6=#7F:
R8=3 ON LINE 0 : FRAME SIZE=#2C20 usec (R9=7)(R7=0)
R8=3 ON LINE 1 : FRAME SIZE=#2C00 usec (R9=7)(R7=0)
R8=3 ON LINE 2 : FRAME SIZE=#2C60 usec (R9=7)(R7=0)
R8=3 ON LINE 3 : FRAME SIZE=#2C40 usec (R9=7)(R7=0)
R8=3 ON LINE 4 : FRAME SIZE=#2CA0 usec (R9=7)(R7=0)
R8=3 ON RASTER LINE 2 / R0=0 ON LINE 43 / FRAME SIZE=#4600 usec (R9=7)(R7=0)
R7=#18, BEFORE R6
CALC WITH R6=#19:
R8=3 ON LINE 0 : FRAME SIZE=#1B00 usec (R9=7)(R7=0)
R8=3 ON LINE 1 : FRAME SIZE=#1B40 usec (R9=7)(R7=0)
R8=3 ON LINE 2 : FRAME SIZE=#1B40 usec (R9=7)(R7=0)
R8=3 ON LINE 3 : FRAME SIZE=#1B80 usec (R9=7)(R7=0)
R8=3 ON LINE 4 : FRAME SIZE=#1B80 usec (R9=7)(R7=0)
R8=3 ON RASTER LINE 2 / R0=0 ON LINE 43 / FRAME SIZE=#2800 usec (R9=7)(R7=0)
```


CRTC 4 INTERLACE VIDEO MODE

RR UPDATE DELAY + 0 FRAME DELAY

RR=3 ON C9=0, C0=#3D : FRAME SIZE=#2C00 usec (R9=7)
RR=3 ON C9=0, C0=#3E : FRAME SIZE=#2C20 usec (R9=7)
RR=3 ON C9=0, C0=#3F : FRAME SIZE=#2C00 usec (R9=7)
RR=3 ON C9=1, C0=#00 : FRAME SIZE=#2C00 usec (R9=7)
RR=3 ON C9=1, C0=#01 : FRAME SIZE=#2C20 usec (R9=7)

RR UPDATE DELAY + 0 FRAME DELAY

RR=3 ON C9=0, C0=#3D : FRAME SIZE=#2C20 usec (R9=7)
RR=3 ON C9=0, C0=#3E : FRAME SIZE=#2C00 usec (R9=7)
RR=3 ON C9=0, C0=#3F : FRAME SIZE=#2C20 usec (R9=7)
RR=3 ON C9=1, C0=#00 : FRAME SIZE=#2C20 usec (R9=7)
RR=3 ON C9=1, C0=#01 : FRAME SIZE=#2C00 usec (R9=7)

RR UPDATE DELAY + 1 FRAME DELAY

RR=3 ON C9=0, C0=#3D : FRAME SIZE=#2C00 usec (R9=7)
RR=3 ON C9=0, C0=#3E : FRAME SIZE=#2C20 usec (R9=7)
RR=3 ON C9=0, C0=#3F : FRAME SIZE=#2C00 usec (R9=7)
RR=3 ON C9=1, C0=#00 : FRAME SIZE=#2C00 usec (R9=7)
RR=3 ON C9=1, C0=#01 : FRAME SIZE=#2C20 usec (R9=7)

DELAY FOR EVEN+ODD FRAME (E/O R6=50/50, 7F/50, 50/7F, 7F/7F)

RR=3 ON LINE 0 : FRAME SIZE=#57C0 usec (R9=7)(R7=0)
RR=3 ON LINE 0 : FRAME SIZE=#57C0 usec (R9=7)(R7=0)
RR=3 ON LINE 0 : FRAME SIZE=#57C0 usec (R9=7)(R7=0)
RR=3 ON LINE 0 : FRAME SIZE=#57C0 usec (R9=7)(R7=0)

INTERLACE C4/C9 COUNTERS

CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM

- (1) INTERLACE C4/C9 COUNTERS
- (2) INTERLACE CRTC 2 C9 STRANGER THING
- (3) FAKE USYNC ON CRTC 2
- (4) CRTC 2 FIND C0 MIN
- (5) CRTC 2 RLAL
- (6) CRTC 1 BUG OUTI R0

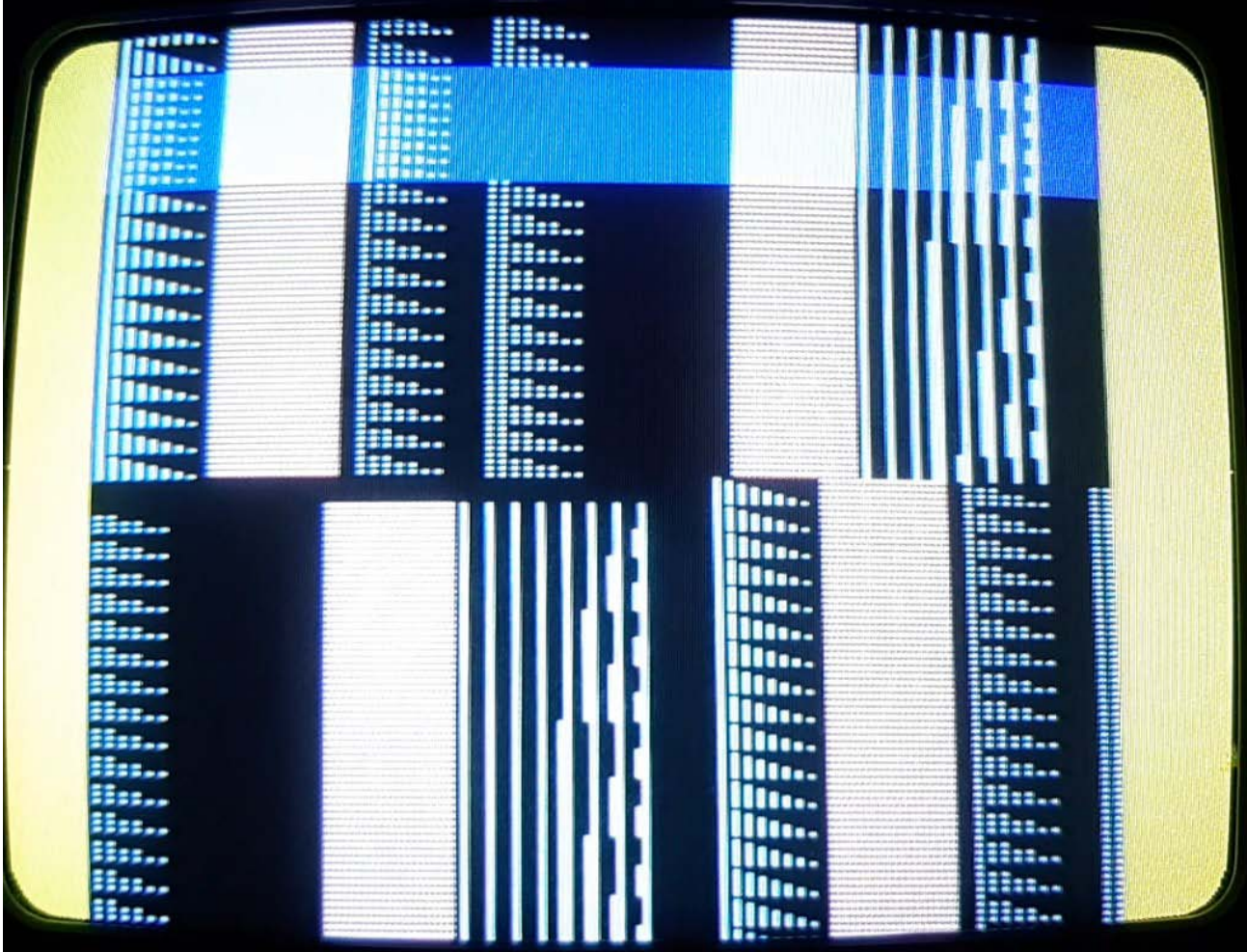
(S) BE00 CHECK (CRTC 1)

(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT (<) CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC USYNC SET PPI.PORTB.0=1 !!

CRTC 4 INTERLACE VM TESTS - C4/C9 COUNTING IN IVM PERIOD (MAJUE ZONE)

NEXT SCREEN : C4=6, C9=0 >> UPD R9=6, R8=3 (+3105)
EXIT IVM MODE ON C9=0 >> UPD R9=7, R8=0

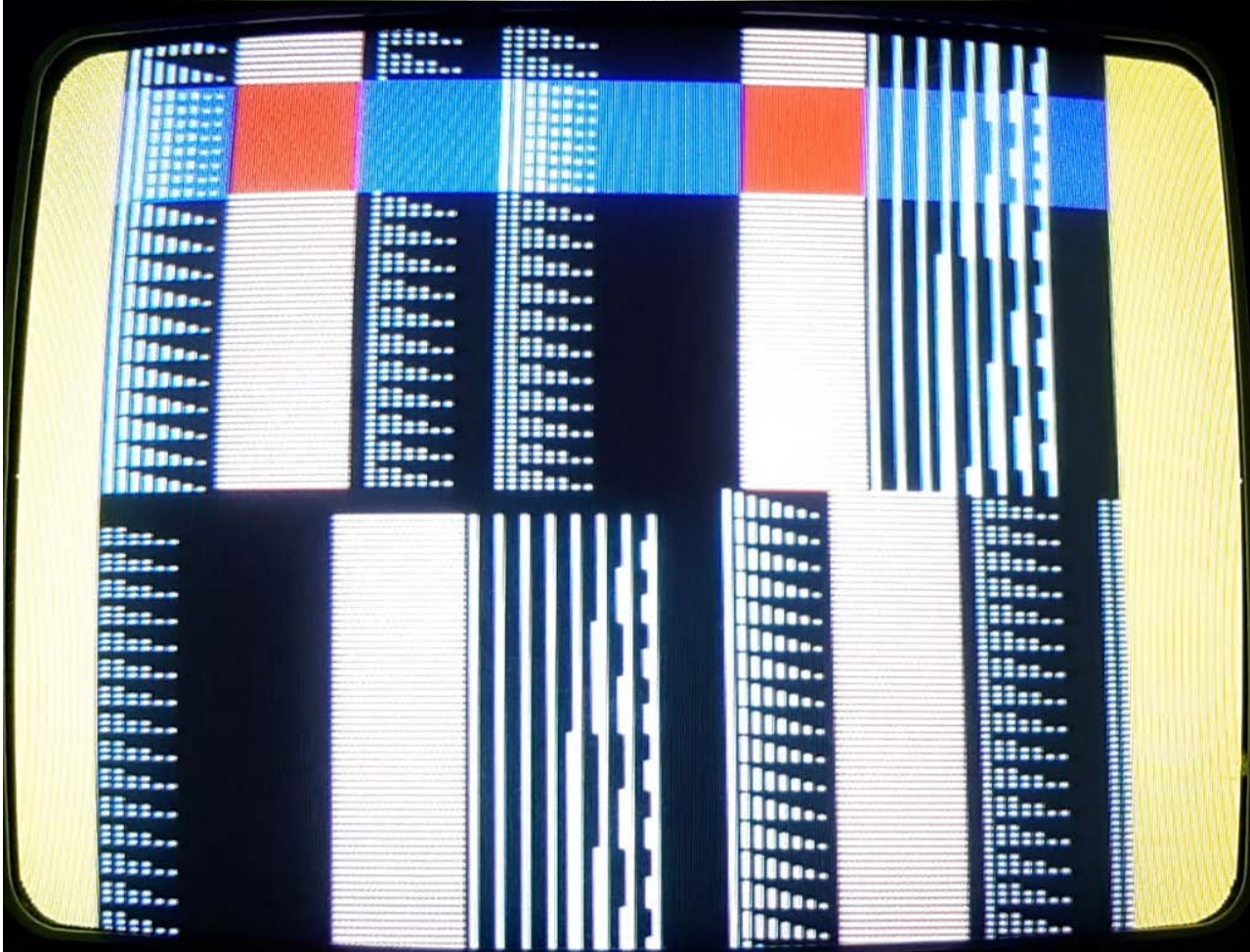
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=0x0x R5=0x0x



CRIC 4 INTERLACE VM TESTS - C4/C9 COUNTING IN ION PERIOD (HARVE ZONE)

NEXT SCREEN : C4=6, C9=1 >> UPD R9=6, R8=3 (+310S)
EXIT ION MODE ON C9=0 >> UPD R9=7, R8=0

AUTOSYNC ON PREVIOUS SCREEN TEST: R4=02A R5=000

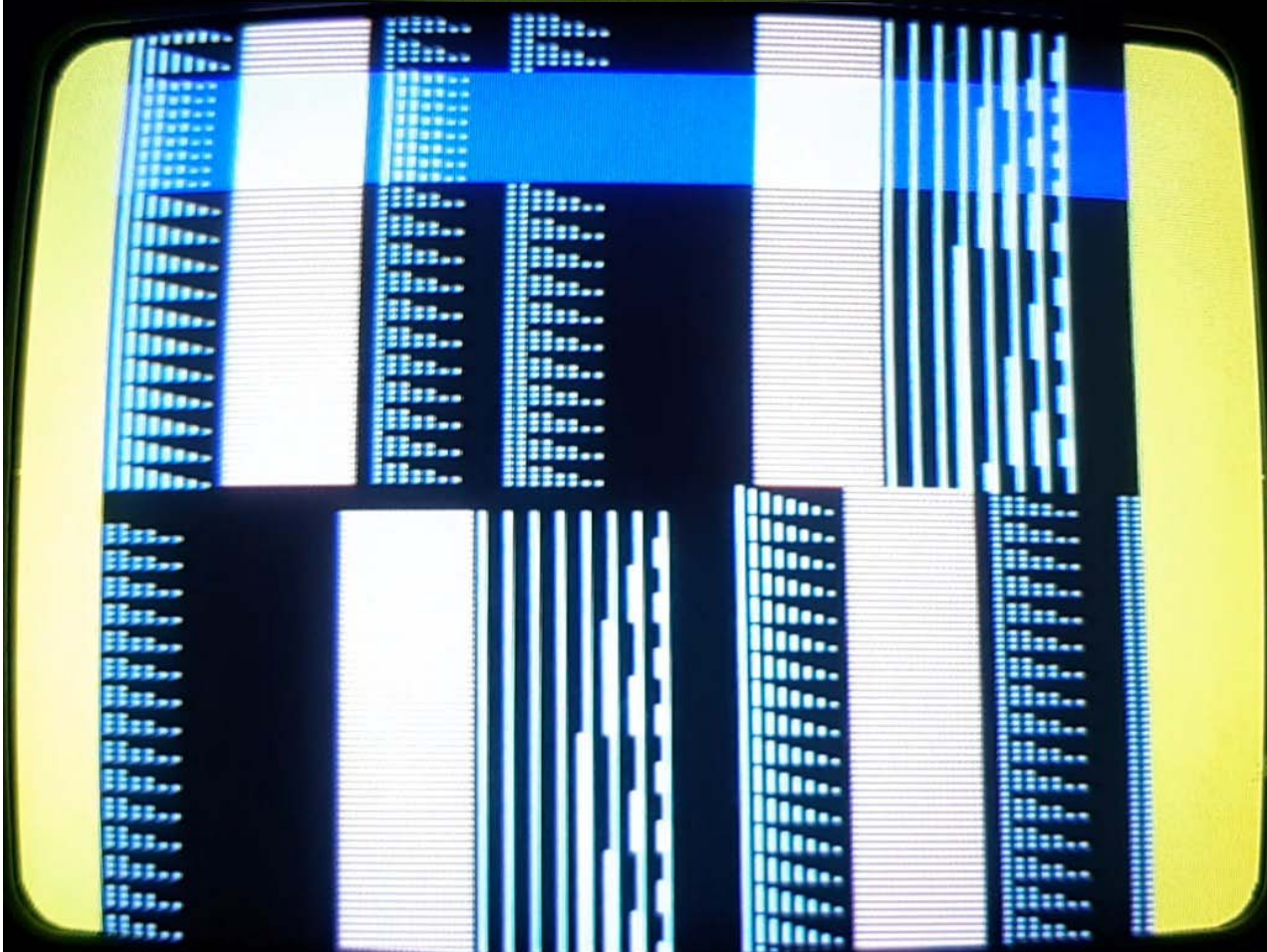


CHIC 4 INTERLACE VM TESTS - C4/C9 COUNTING IN ION PERIOD (HARD ZONE)

NEXT SCREEN : C4-6, C9-2 >> UPD R9-6, R8-3 (+3105)

EXIT ION MODE ON C9-0 >> UPD R9-7, R8-0

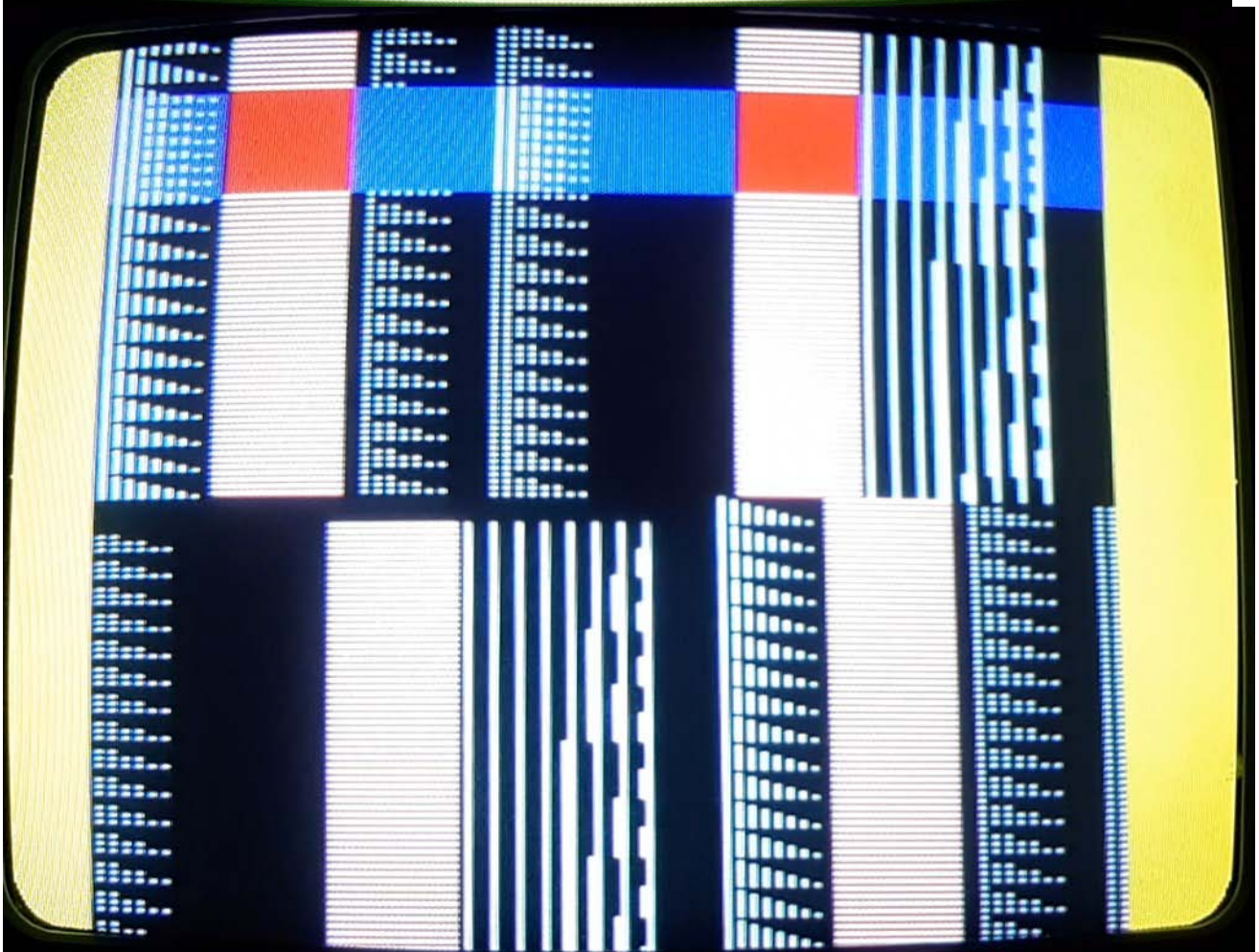
AUTOSYNC ON PREVIOUS SCREEN TEST: R4-029 R5-007



CRTC 4 INTERLACE ON TESTS - C4/C9 COUNTING IN IOM PERIOD (MAUVE ZONE)

NEXT SCREEN : C4=6, C9=3 >> UPD R9=6, R8=3 (+310S)
EXIT IOM MODE ON C9=0 >> UPD R9=7, R8=0

AUTOSYNC ON PREVIOUS SCREEN TEST: R4=R29 R5=R07

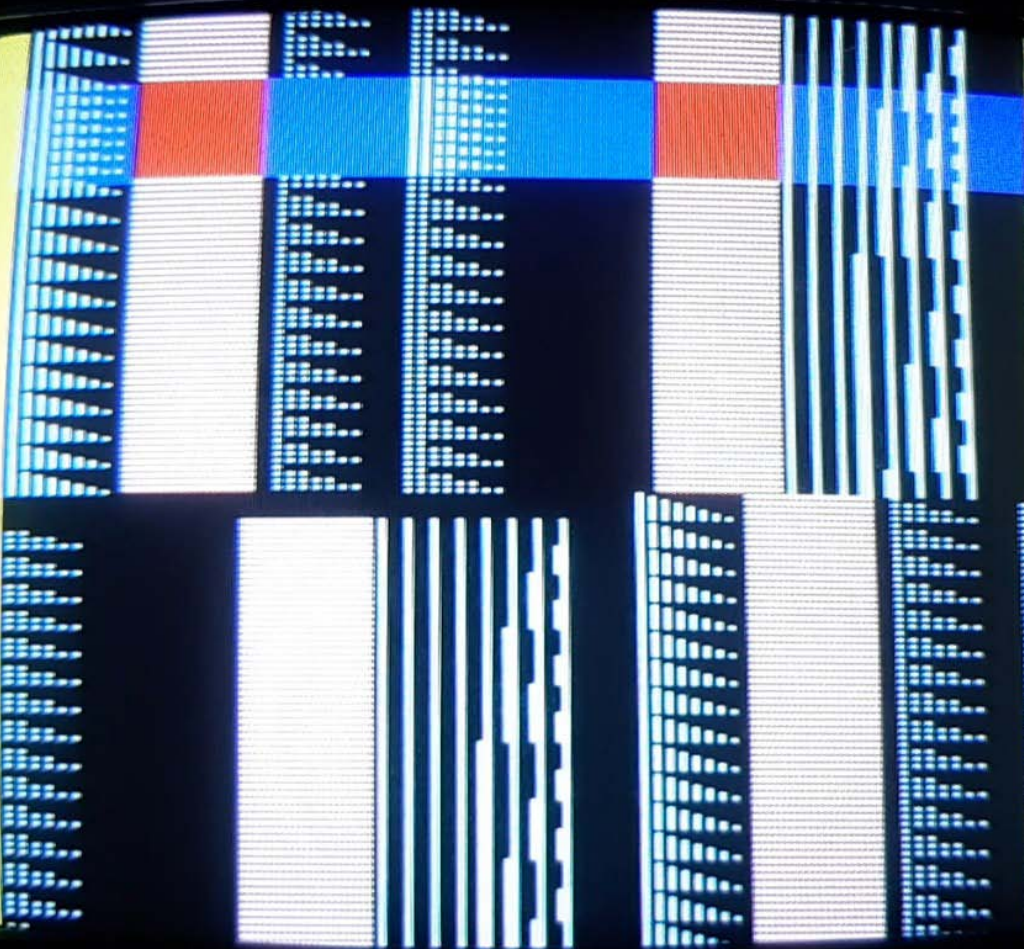


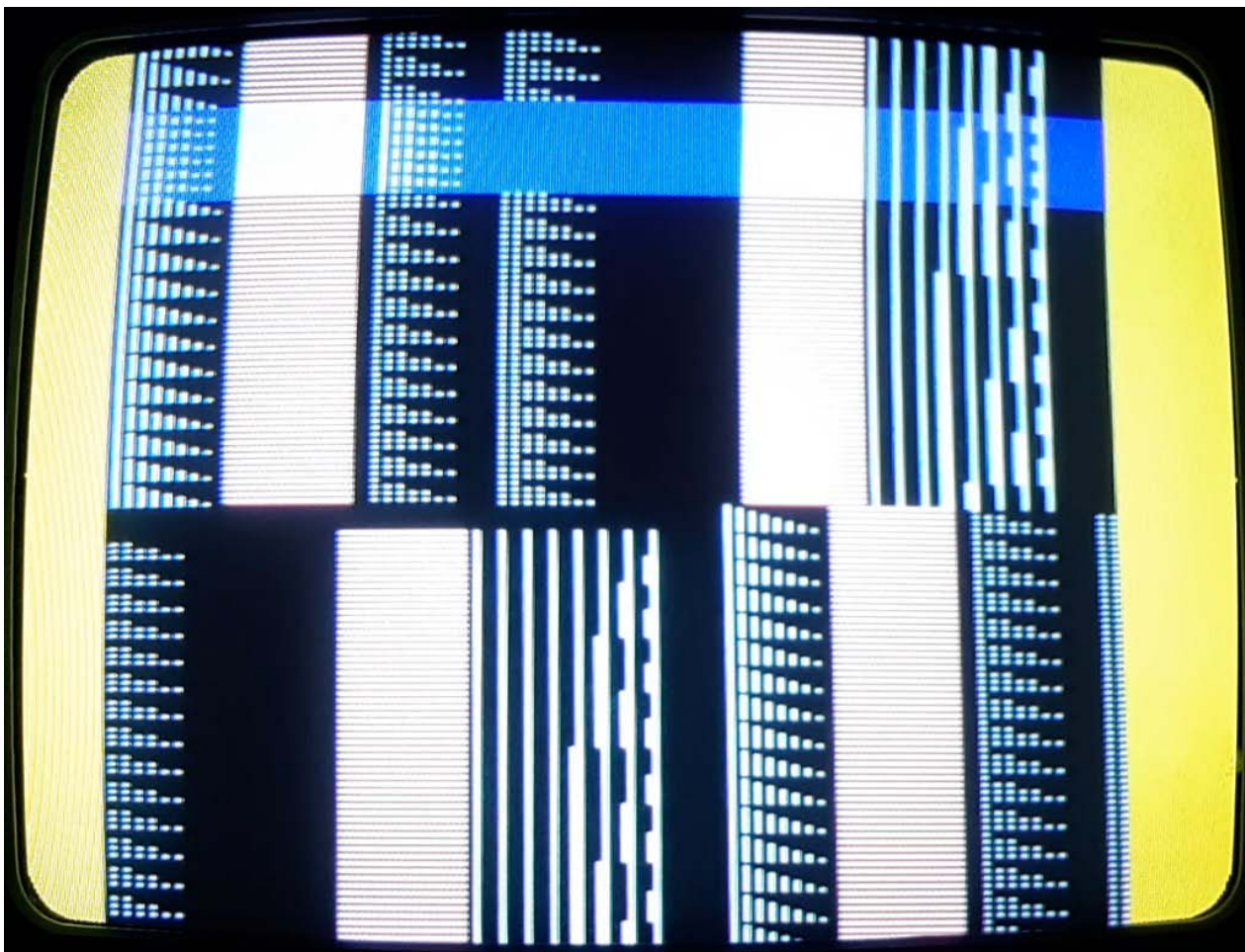


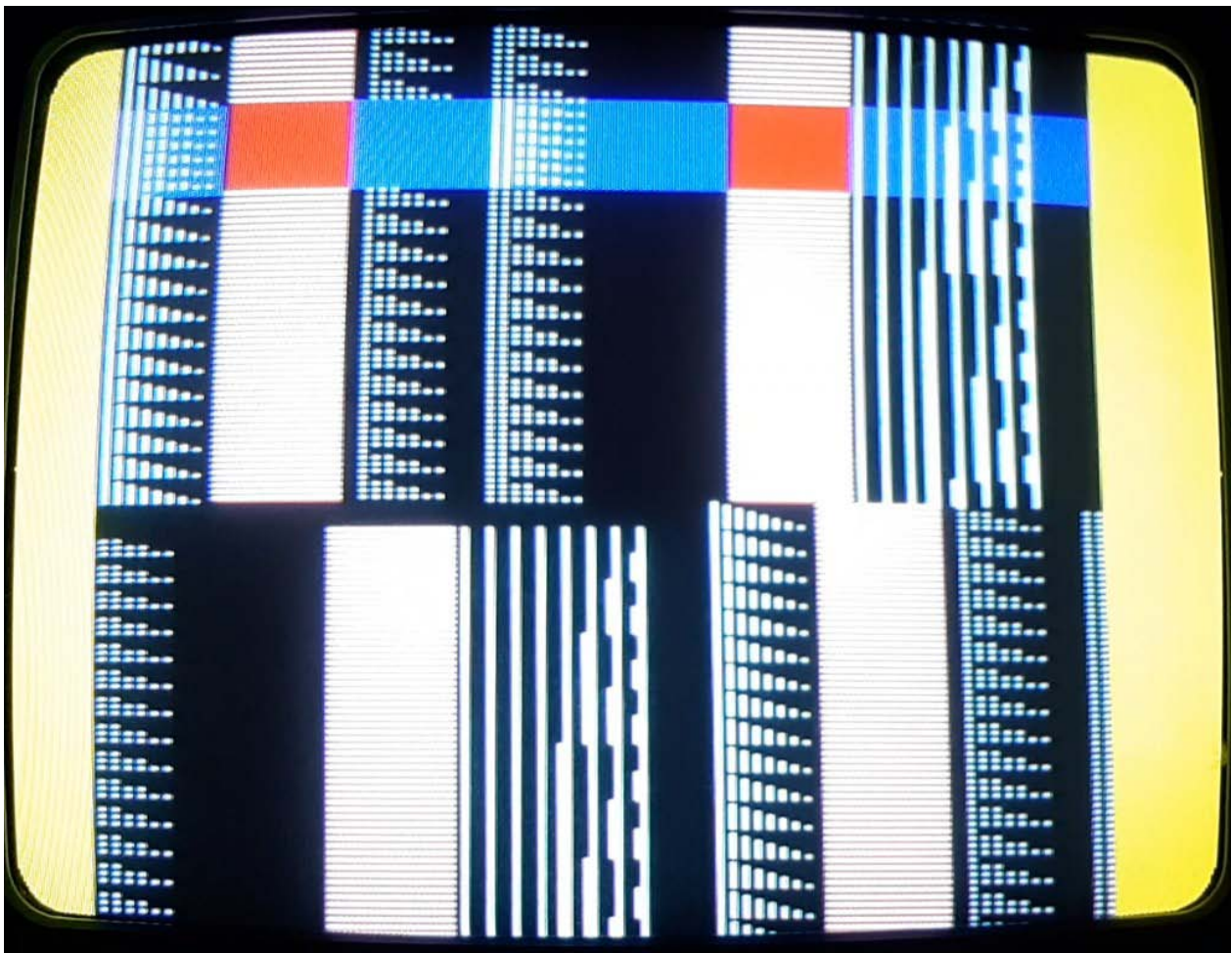
CRYC 4 INTERLACE VM TESTS - C4/C9 COUNTING IN IVM PERIOD (HAQUE ZONE)

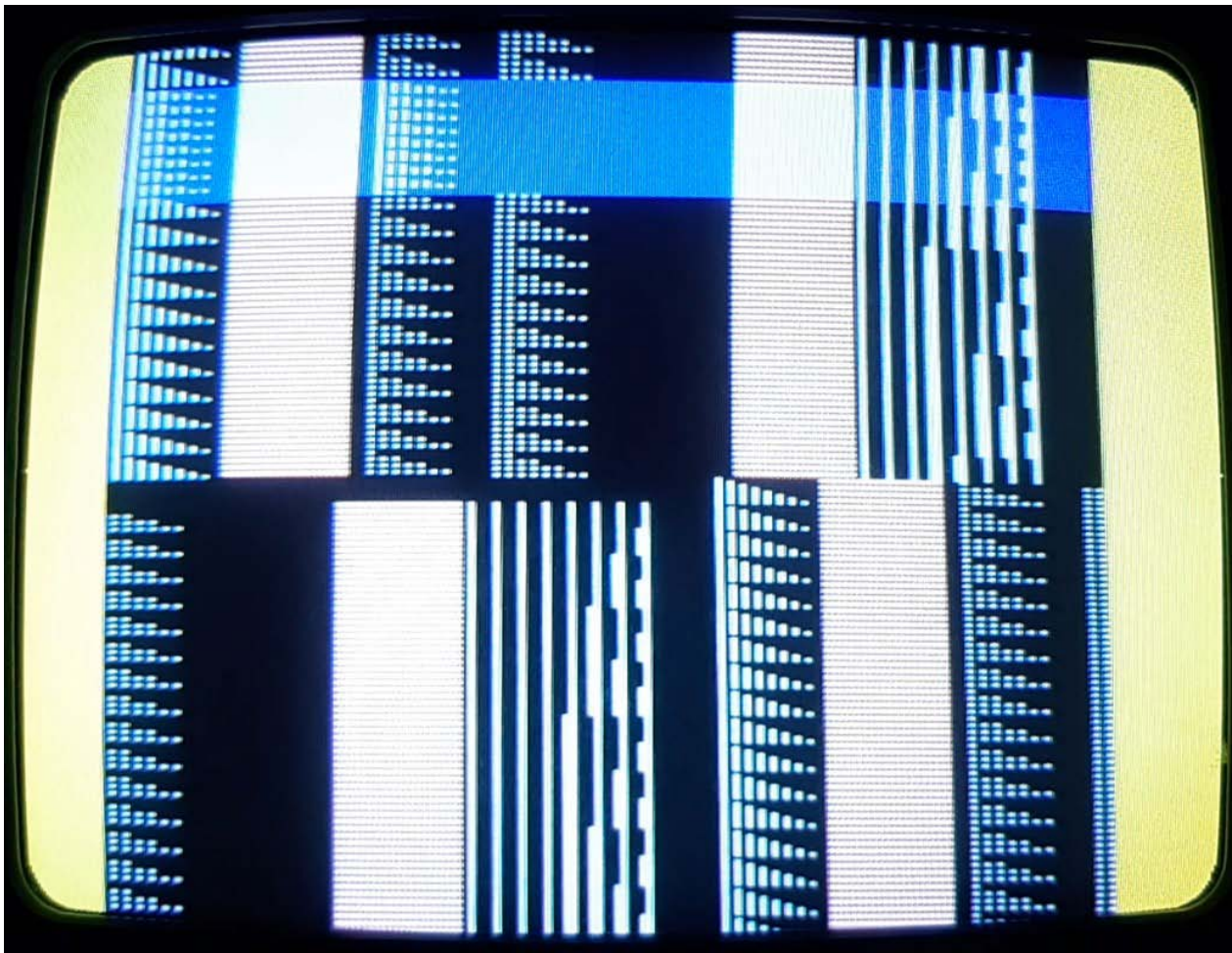
NEXT SCREEN : C4=6, C9=5 >> UPD R9=6, R8=3 (+310S)
EXIT IVM MODE ON C9=0 >> UPD R9=7, R8=0

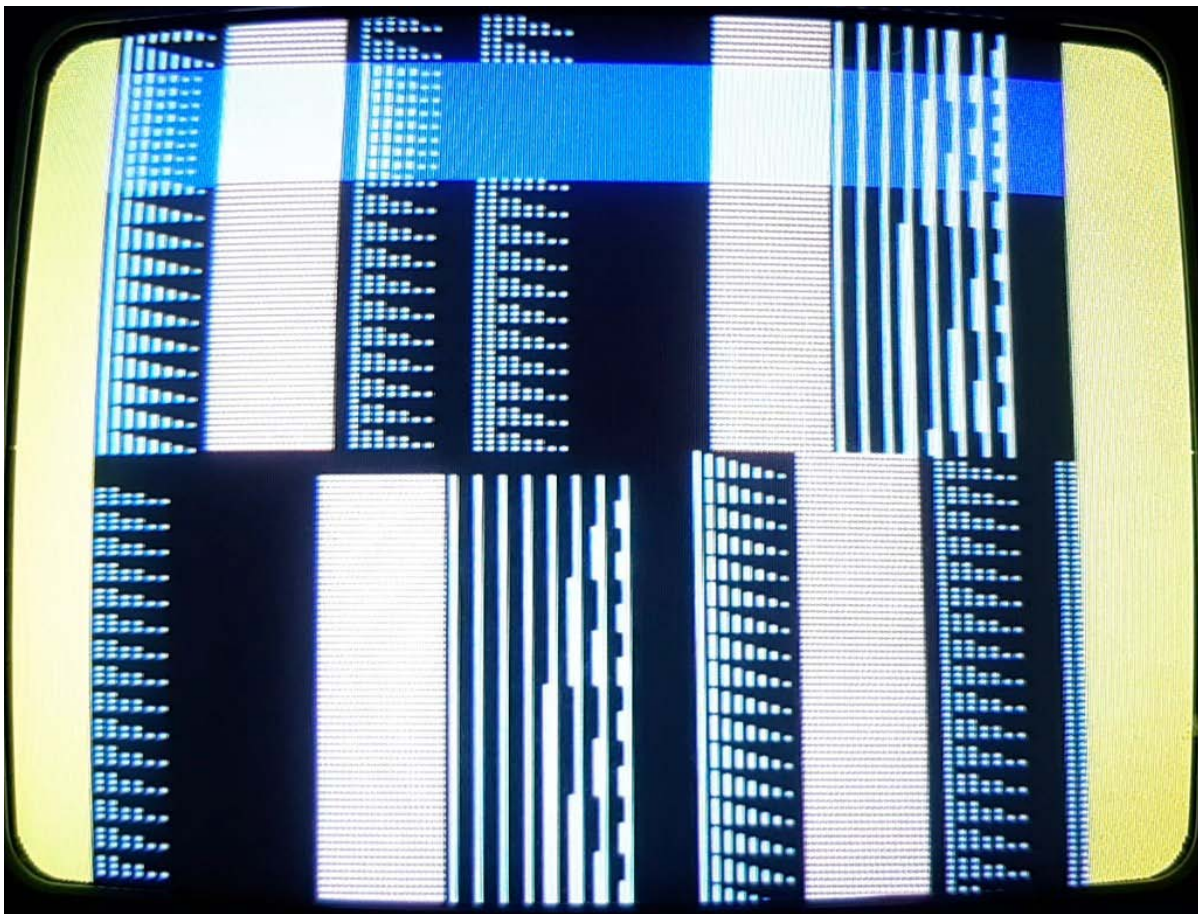
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=029 R5=004

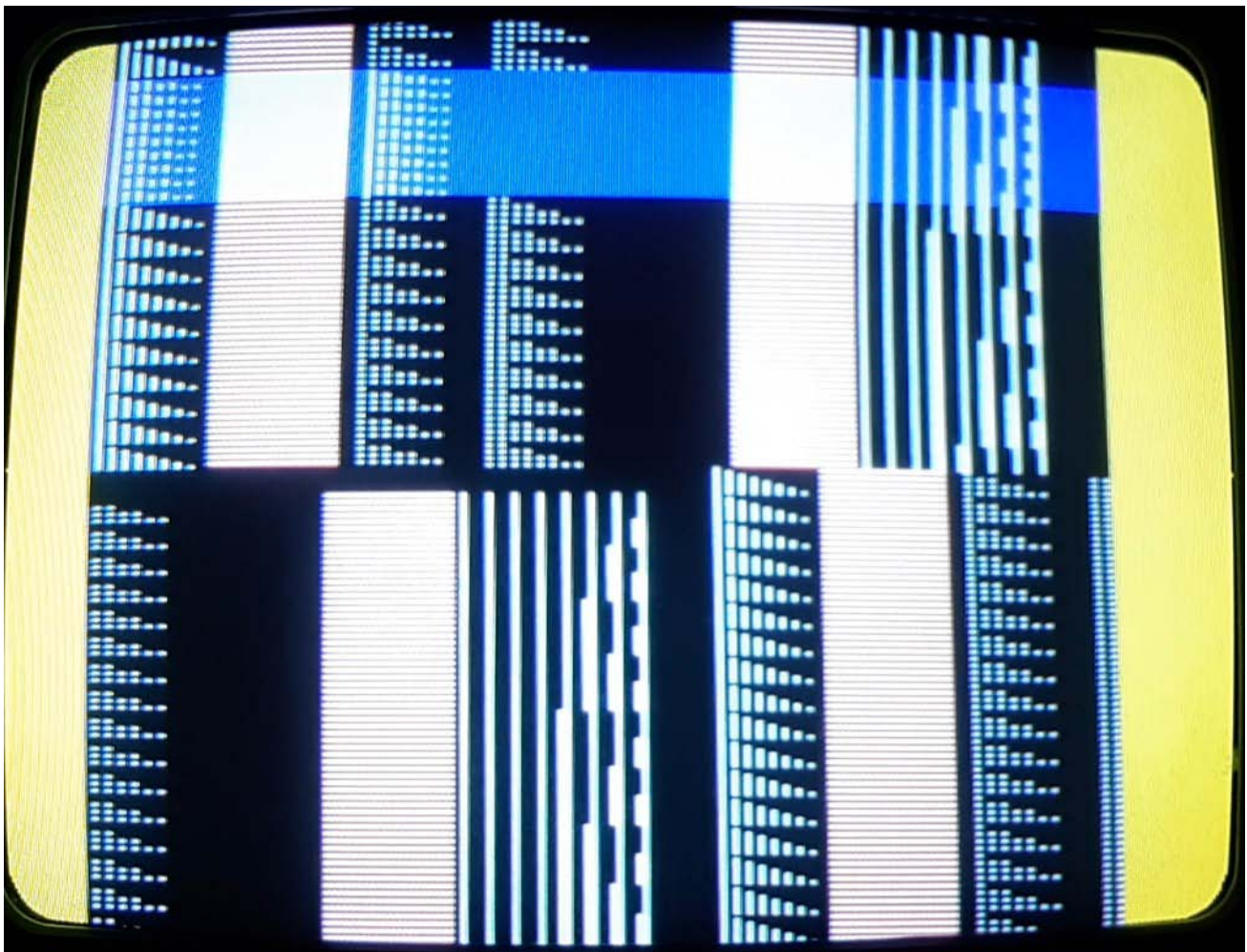












INTERLACE CRTC 2 C9 STRANGER THING

CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT, LOGON SYSTEM

- (1) INTERLACE C4/C9 COUNTERS
- (2) INTERLACE CRTC 2 C9 STRANGER THING
- (3) FAKE VSYNC ON CRTC 2
- (4) CRTC 2 FIND C0 MIN
- (5) CRTC 2 RLAL
- (6) CRTC 1 BUG OUTI R0

(S) BE00 CHECK (CRTC 1)

(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT (<) CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC VSYNC SET PPI.PORTB.0=1 !!

Only for CRTC 2

FAKE VSYNC ON CRTC 2

CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM

- (1) INTERLACE C4/C9 COUNTERS
- (2) INTERLACE CRTC 2 C9 STRANGER THING
- (3) FAKE VSYNC ON CRTC 2
- (4) CRTC 2 FIND C0 MIN
- (5) CRTC 2 RLAL
- (6) CRTC 1 BUG OUTI R0

(S) BE00 CHECK (CRTC 1)

(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT (<>) CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC VSYNC SET PPI.PORTB.0=1 !!

TRYING FAKE VSYNC VIA PPI PORT B MIDDLE SCREEN
FAKE VSYNC OK IF VSYNC BLACK BAND

CRTC 4

CRTC 2 FIND C0 MIN

CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM

- (1) INTERLACE C4/C9 COUNTERS
- (2) INTERLACE CRTC 2 C9 STRANGER THING
- (3) FAKE USYNC ON CRTC 2
- (4) CRTC 2 FIND C0 MIN
- (5) CRTC 2 RLAL
- (6) CRTC 1 BUG OUTI R0

(S) BE00 CHECK (CRTC 1)

(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT (<) CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC USYNC SET PPI.PORTB.0=1 !!

Only for CRTC 2

CRTC 2 - 1 LINE RUPTURE

CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM

- (1) INTERLACE C4/C9 COUNTERS
- (2) INTERLACE CRTC 2 C9 STRANGER THING
- (3) FAKE USYNC ON CRTC 2
- (4) CRTC 2 FIND C0 MIN
- (5) CRTC 2 RLAL
- (6) CRTC 1 BUG OUTI R0

(S) BE00 CHECK (CRTC 1)

(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT (<) CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC USYNC SET PPI.PORTB.0=1 !!

Only for CRTC 2

CRTC 1 - BUG OUTI R0

CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM

- (1) INTERLACE C4/C9 COUNTERS
- (2) INTERLACE CRTC 2 C9 STRANGER THING
- (3) FAKE USYNC ON CRTC 2
- (4) CRTC 2 FIND C0 MIN
- (5) CRTC 2 RLAL
- (6) CRTC 1 BUG OUTI R0

(S) BE00 CHECK (CRTC 1)

(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT (<) CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC USYNC SET PPI.PORTB.0=1 !!

CHECKING BUG OUTI ON RB UPDATE WHEN C0=0
ON C4=C9=0, 1ST RB=49/2ND RB 'OUTI'=6 FOR 14 usec ON C0vs=46
CRTC 4

CHECKING BUG OUTI ON RB UPDATE WHEN C0=0
ON C4=C9=0, 1ST RB=49/2ND RB 'OUTI'=6 FOR 14 usec ON C0vs=46
CRTC 4

CHECKING BUG OUTI ON RB UPDATE WHEN C0=0
ON C4=C9=0, 1ST RB=49/2ND RB 'OUTI'=6 FOR 14 usec ON C0vs=46
CRTC 4

CHECKING BUG OUTI ON R8 UPDATE WHEN C8=0
ON C4=C9=0, 1ST R8=49/2ND R8 'OUT(C),r8'=6 FOR 14 usec ON CBus=48
CRIC 4

CHECKING BUG OUTI ON R8 UPDATE WHEN C8=0
ON C4=C9=0, 1ST R8=49/2ND R8 'OUT(C),r8'=6 FOR 14 usec ON CBus=48
CRIC 4

CHECKING BUG OUTI ON R8 UPDATE WHEN C8=0
ON C4=C9=0, 1ST R8=49/2ND R8 'OUT(C),r8'=6 FOR 14 usec ON CBus=48
CRIC 4

CRTC 1- BE00 CHECK

```
CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM  
(1) INTERLACE C4/C9 COUNTERS  
(2) INTERLACE CRTC 2 C9 STRANGER THING  
(3) FAKE USYNC ON CRTC 2  
(4) CRTC 2 FIND C0 MIN  
(5) CRTC 2 RLAL  
(6) CRTC 1 BUG OUTI R0
```

```
(S) BE00 CHECK (CRTC 1)
```

```
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT (<>) CRTC CAR DISPLAY  
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC USYNC SET PPI.PORTB.0=1 !!
```

Only for CRTC 1